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DISTANCE PROTECTION: OPTIMUM DYNAMIC DESIGN OF STATIC RELAY COMPARATORS

S y n o p s i s

The ease with which transistor comparators for distance relays can be designed for high-speed operation must be tempered with consideration of overall performance and integrity of operation. Operating speed must be defined over the whole of the working range of the relay, and neither the speed nor the measuring accuracy should be unduly affected by the severe transients generated by modern e.h.v. networks. The comparator, as well as being proof against damaging voltage surges, must operate accurately in the presence of long-duration offset transients accentuated by low-loss modern-plant parameters and the random point-on-wave inception of faults due to natural hazards and closure or reclosure of modern pressure-head circuit breakers. The attainment of high-speed operation under these practical conditions precludes the adoption of many, apparently practical transistor-comparator circuits and favours the adoption of circuits with well defined dynamic performances.

Extensive laboratory investigation has shown that the block-average comparison principle is amenable to precise design in all respects, and practical fast-operating relays can be designed with good transient-free characteristics. The results obtained on such a practical relay are presented in the paper for a phase comparator with a polarised-mho characteristic. It is shown that a minimum inherent

operating time of one halfcycle of the power frequency can be defined for this comparator arrangement and that both the static and dynamic operating characteristics are predictable over the whole working range. Equivalent performance for the amplitude-comparator counterpart is justified in an appendix, and underlines earlier work.

Relays using the block-average comparison principle have been used successfully in field trials since 1957, and this principle now forms the basis for various production designs. Sufficient field experience is now available to justify the theoretical analysis and laboratory test results given in the paper.

LIST OF PRINCIPAL SYMBOLS

V_1, V_2 - input signals to a 2-input relay comparator
ϕ - phase displacement between V_1 and V_2
V_L - phase-to-phase voltage
I_L - line current
V_{s1}, V_{s2} - level-detector voltage settings
S_1 - p.u. input 1 related to setting
S_2 - p.u. input 2 related to setting
V_x, V_y - particular levels of voltage in a level detector, corresponding to time intervals T_x and T_y, respectively
V_p - polarising voltage
T - system periodic time
α - phase-comparator angular setting
$Z_L = V_L/I_L$ - protected impedance of a section of power system
Z_R - relaying-system impedance setting

1. Introduction

Until a decade ago, relay design was dominated by the use of electromechanical elements. Such an element, of whatever basic characteristis; e,g. square-law induction element, has a dynamic behaviour special to that element, and design freedom is consequently restricted by factors such as the conflicting requirements of sensitivity and mechanical robustness. The same period saw the emergence of a method for assessing the dynamic performance of different relaying systems by displaying timing contours under practical conditions of switching [5]. The relative deficiencies of several types of relay could thus be exposed, and criteria for dynamic performance be established. Furthermore, it became possible to establish correlation between operating time, switched measuring accuracy and overall integrity under practical operating conditions. Over the last ten years, relays using transistors have been shown to be practical alternatives to relays using conventional co components [1-4] and both phase and amplitude comparators have been used with double and multiple inputs. Although the relationships of geometrical duality between phase- and amplitude-comparators in the steady state are well established [7], the respective dynamic performances have not been adequately rationalised.

The transistor comparator affords great freedom of design for specific laws of operation and/or characteristics; this has no counterpart in the electromechanical relay, where the basic characteristics are prescribed by the behaviour of the element itself. This freedom of design embraces both static characteristics and dynamic performance. Rationalisation beyond elementary reproduction of conventional dynamic performance becomes possible, design procedure is clarified, and the relative assessment of comparators operating to different principles is facilitated.

The transformation of input quantities defining identical steady-state operating characteristics using phase or amplitude comparators is shown below to have extended significance in rationali-

sing comparator performance, especially in the case of circuits using transistors.

2. Design principles of transistor distance relays

2.1. Basis for design

A transistor relay may be designed to have a wide range of different characteristics. These include, on the one hand, a close approximation to an electromagnetic square-law comparator [6] such as the induction cup or balanced-beam type or, on the other hand, a characteristic not normally obtainable by conventional means, such as an inverse relationship between operating time and comparator output. Equally, nonlinear timing relationships can be obtained. It is, in any case, illogical to emphasise the reproduction of conventional-relay characteristics without reconsideration based on the newly available design freedom using transistors. Both inverse and inverse-square timing characteristics arise in conventional relays, because they are inherent to the electromechanical elements used and not because they are necessarily desirable in a functional sense. Reproduction of existing characteristics in this way can lead to unwarranted circuit complexity, without leading to timing or other characteristics which are specially suited to power-system protection requirements. From broad consideration of these protective requirements, it is the authors' opinion (and a view which appears to have majority support among those engineers inimately concerned with protection design and application), that a definite time characteristic is the most desirable one.

Finally, however, it is necessary to assess a relay design beyond the philosophical factors discussed above. Purely technological design aspects, such as long-term circuit stability, susceptibility to damaging transient surges, economic feasibility and performance under nonideal system conditions have influences which often redirect design thinking away from the narrow requirements of the laboratory prototype.

2.2. Phase-comparison and amplitude-comparison

Notwithstanding the fact that Ellis [7,8] established that there were no fundamental differences between these two principles, unfounded comparisons have been made. For example, Mathews and Nellist [9] presented an analysis of the differential rectifier-bridge comparator and mentioned its inferior transient response relative to the transistor phase comparator described by Adamson and Wedepohl [2]. In order to clarify this point, it is established in Appendix 9 that with both a basic phase and an amplitude comparator, each with specified operating criteria, the output signals are identical, instant by instant, provided that the correct input relationships specified by Ellis [7] are observed. Thus, the only way in which differences in dynamic performance in the two cases can occur is if there are differences in the passive networks processing the input signals, or in the circuits connected to the comparator output.

2.3. Useful characteristics obtained using transistor comparators

There is little doubt that some of the past uncertainties concerning electromechanical relays have resulted from ill-considered attempts to compare the inherent performance of phase comparators and amplitude comparators with fundamentally different output characteristics, e.g. a linear moving-coil element compared with a square-law induction-cup element. With transistor relays, similar misconceptions can arise, and it is important to recognise that the number of basically different methods of obtaining useful characteristics from a comparator circuit is confined to the following:

a) Block instantaneous comparison [1] in which the duration of polarity coincidence determines the output. The tripping criterion is that the duration of the first coincidence should exceed a specified time, usually one quarter of the power-frequency period.

b) Block average comparison, a development of (a), in which the duration of polarity coincidence is measured on both halfcycles of the input signals, and the average value is determined in an integrating circuit, a trip signal being produced if a specified average value is maintained for more than a prescribed duration. The principles of this form of comparison have already been described [2,3,10] .

c) Pulse comparison [1], in which the polarity of one signal is measured during a short interval in the cycle of the second signal, usually, but not necessarily, at the latter's peak.

Whether a practical transistor comparator in categories a) or (b) is based on phase or amplitude compararison has been shown to be immaterial. To date, practical comparators falling into category (c) are of the phase-comparison type only, even though equivalent amplitude versions can be conceived. Thus, the relative merits of practical comparators of each category are conveniently compared by considering phase-angle comparators only, in detail. This choice has practical significance in that the inherent characteristics of transistors lend themselves most readily to phase-comparator principles.

2.4. Fundamental principles of operation of transistor comparators

Considering phase comparators in the three categories of Section 2.3, the operating criterion is expressed in the equation:

$$-\alpha \leqslant \phi \leqslant +\alpha \qquad (1)$$

where ϕ is the phase difference between the two input signals and α is the phase-angle setting, usually $\pi/2$. For the block comparators of categories (a) and (b), the operating limit α may by preset between 0 and π to give overall characteristics comprising sectors of circles and straight lines in the complex plane [3,]. The case of an operating limit of $\pi/2$ yields characteristics which compri-

se either straight lines or circles[1]. Thus, in the steady state, there are no basic differences between the three comparators, but it can be observed that the block-comparison principle allows for greater versatility.

Consideration of relative dynamic performance discloses sharper contrasts, however. Comparators in the first and last category are inherently susceptible to system transients and other spurious signals by virtue of their near instantaneous operation[1,2]. Unless all unwanted surges and transients are effectively removed from the signal inputs, their measuring accuracy cannot be maintained under dynamic conditions without sacrifice in operating speed. A compromise solution has been proposed 2 wherein two identical comparators are arranged to compare signals on alternate halfcycles, and their outputs are gated so that trasient overreach in one element is blocked by the other. Other arrangements use"first-block-rejection"circuits [11] or "gap-timing" circuits. All such attempts to preserve dynamic measuring accuracy sacrifice speed of operation, because the form of comparator with which they are associated have no inherent trasient-free characteristics.

The block-average comparator, however, has useful inherent transient-free characteristics, and it is shown in the following Sections that a relay can be designed to a theoretical minimum operating time of one half of the power-frequency period without incurring transient overreach and without resorting to special filtering circuits in the input signal paths. The operating time is not significantly affected by the instant of fault initiation or degree of the d.c. offset transient in the input signals, and can be precisely defined following the procedure described in Section 3. Timing over the full working range approaches the ideal definite-time characteristic, but as the critical phase angle α(usually$\pi/2$) is approached, the timing tends to infinity at the boundary of operation. This controlled timing-characteristic, and the use of both halfcycles for measurement, contribute most significantly to the dynamic accuracy, and contrasts with the other two types of compa-

rator with their variation in timing depending on the point-on-wave instant of fault initiation and the uncontrolled timing characteristic at or near the boundary of operation. This latter property largely accounts for their poor dynamic measuring properties and for their susceptibility to maloperation resulting from spurious surges and transient signals; the comparators in categories(a) and (c) are probably of lowest merit in these respects.

3. Block average comparison

3.1. Specification of design requirements

The following are the factors of most significance in relating inherent comparator performance to the conjunctive performance of any practical distance-measuring relay and, as such, they are used as the basis for specifying the blockaverage system:

a) Measuring accuracy: The specified accuracy should be maintained over the full working range when measured under realistic dynamic conditions with offset d.c. transients and other spurious signals superimposed on the input quantities. Long-term stability of measuring accuracy requires that the comparator design levels be such that all vectorial signal mixing should be done in passive circuits before the signals are compared.

b) Timing characteristic: The timing characteristic should be of the definite-minimum type for all faults within the protected zone, allowance being made for controlled performance in the immediate vicinity of the operating boundary. An operating time of the order of 1 cycle of power frequency is considered desirable over the majority of the practical working range.

c) Stability: The comparator should have inherent resistance to high-amplitude short-duration system-generated surges,both with regard to maloperation and to surge damage.

It is of fundamental importance in developing a sound relaying philosophy to consider in close detail the inherent performance as set out above, bearing in mind that modern high-speed relays, are required to operate correctly in the presence of long-duration offset d.c. transients. The major part of any discussion on performance must thus centre on the dynamic response of the relay and on its operating mechanism in the presence of offset d.c. components, with the clear understanding that the steady-state response is merely a particular case of the dynamic response. It is on this basis that relays using the principle of block-average comparison are at an advantage over simpler adn/or faster arrangements in which design is based on steady-state considerations only.

3.2. Basic considerations

Fig. 1 shows a schematic diagram of a basic relay using the phase-comparator principle: the definitive equations can be derived

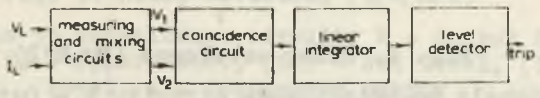

Fig. 1. Basic block average comparison relay

and performance will be identical for an equivalent amplitude comparator. Two input quantities V_1 and V_2, derived from input voltage and current V_L and I_L in a measuring and mixing circuit, are compared in a coincidence circuit producing standard output pulses, which are positive when V_1 and V_2 are of the same polarity and negative when they are of opposite polarity. The pulses are applied to an integrating circuit whose output increas s linearly during the time when the pulse is positive and falls at the same rate when the polarity reverses. The final element in the relay is a level detector which switches when the integrator output

exceeds some preset value, and resets when the output falls below some second value.

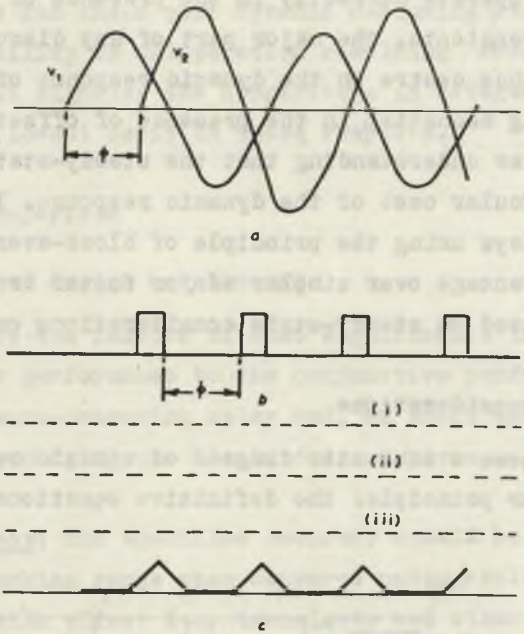

Fig. 2. Relay waveforms ($\phi > \pi/2$)

a - Input signals to coincidence circuit, b - Output from coincidence circuit (i) - Upper limit, (ii) Set level, (iii) - Reset level, c- Integrator output

Figs. 2 and 3 show the relevant waveforms in the steady state for phase displacements $\phi > \pi/2$ and $\phi < \pi/2$, respectively. It is evident that the output signal from the integrator is sawtooth in nature, and that there is an effective gain in output only for the condition $\phi < \pi/2$. The rise and fall rates in the integrator are at the designer's disposal, so that the critical phase angle may be set to any desired value. Both the level-detector set and reset levels are critical in relation to the total excursion limit of integrator linearity and also to the slope of the output. Considering first the setting, it may be seen that this should at least exceed a value which would be reached after one quarter of the system pe-

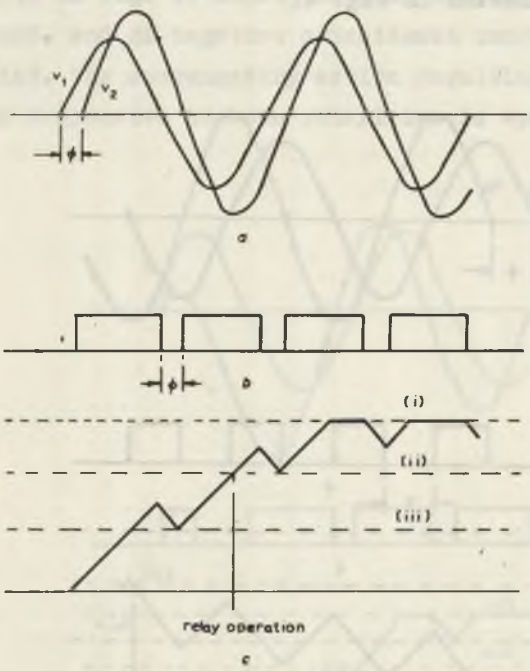

Fig. 3. Relay waveforms ($\phi < \pi/2$)

a - Input signals to coincidence circuit, b - Output from coincidence circuit,-(i) - Upper limit, (ii) - Set level, (iii) - Reset level, c - Integrator output

riodic time. If this were not so, the output would switch at twice system frequency, even if the displacement between input signals was greater than the critical value. The difference between set and reset levels should also exceed this same value in order that cyclic switching does not occur for marginal phase displacements when the net rate of change of integrator output is very small; this is illustrated in Fig. 4. Finally, the upper limit of linearity should not be excessive, otherwise the reset time will be poor.

If all these factors are taken into account, together with the problem of designing a trigger circuit to operate to a specified level, it is found that the optimum level-detector setting is two

thirds of the integrator excursion limit and reset one third of the same limit, as indicated in Fig. 4.

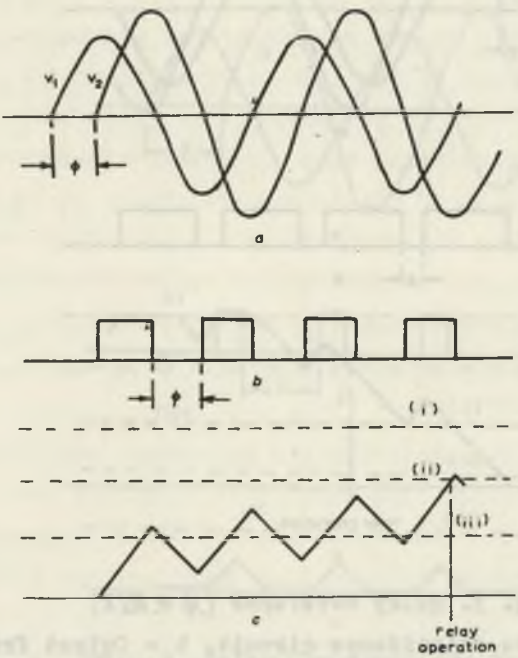

Fig. 4. Relay waveforms for marginal operation ($\phi = \pi/2$)

a - Input signals to coincidence circuit, b - Output from coincidence circuit (i) Upper limit, (ii) Set level, (iii) Reset level, c - Integrator output

3.3. Response time

The basic time-response characteristic is of fundamental importance. Since the response is directly related to the coincidence time, it is a simple matter to derive the equation relating this time (which, in turn, is proportional to the complement of phase displacement, $\pi - \phi$, in the steady state) to the time of operation. The response time is directly related to the time taken for the integrator to produce a signal which actuates the level detector under conditions of continuous coincidence. Under conditions of maximum

d.c. offset transient in one signal, operation can be delayed slightly as shown in Fig. 5, where the time of positive coincidence has been reduced, and of negative coincidence increased, over the transient period. The compensatory action resulting from the use of an integrator responsive to both polarities is apparent.

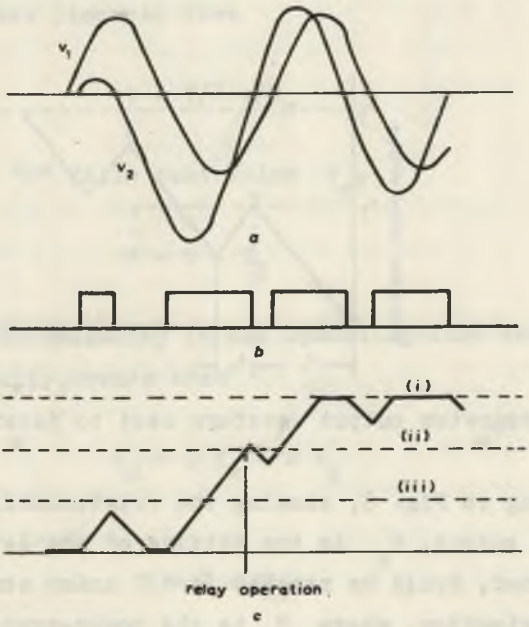

Fig. 5. Relay waveforms with d.c. offset in V_2
a - Input signals to coincidence circuit, b - Output from coincidence circuit, (i) Upper limit, (ii) Set level, (iii) Reset level, c - Integrator output

It is clearly advantageous to have the response time as fast as possible: however, the minimum will be related to the spurious output during conditions of maximum d.c. offset transient. Under conditions of maximum d.c. offset transient in V_2, V_2 will, in the limit, have one polarity only, and it is possible to produce a coincidence pulse of exactly one half of a system period in width, and this will be independent of phase shift. It is essential that this

should not actuate the level detector and hence possibly initiate a spurious tripping pulse. This very simple stabilising criterion sets a limit on minimum operating time; from it the inherent operating charcteristic may be readily derived.

This describes the performance of the relay with a d.c. offset in one input only to the comparator; the more general case of transients in both inputs will be covered later.

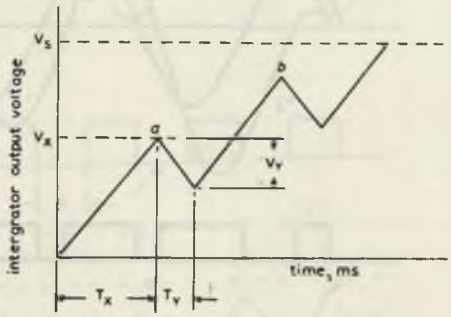

Fig. 6. Integrator output waveform used to determine operating time

Referring to Fig. 6, showing the relationship between time and integrator output, V_s is the setting of the level detector which, it is assumed, would be reached in T/2 under conditions of continuous energisation, where T is the power-system period. Using ϕ for the phase displacement between input signals V_1 and V_2, the following basic equations apply:

$$T_x = (1 - \phi/\pi)T/2 \qquad (2)$$

$$V_x = 2 V_s T_x/T \qquad (3)$$

$$V_y = 2 V_s T_y/T \qquad (4)$$

$$T_x + T_y = T/2 \qquad (5)$$

For zero phase displacement between comparator inputs, point "a" in Fig. 6 coincides with the trigger level V_s, i.e. $V_x = V_s$ and the operating time is T/2. When the point "b" coincides with V_s, the change in integrator output is given by

$$V_s = 2 V_x - V_y \tag{6}$$

and this change takes place in time

$$t = T/2 + T_x \tag{7}$$

If, however, point "b" falls just below V_s,

$$t = T + T_y$$

giving rise to a discontinuity in the operating-time characteristic. The next discontinuity occurs when

$$V_s = 3 V_x - 2 V_y \tag{8}$$

and

$$1 = T + T_x \tag{9a}$$

or

$$3T/2 + T_y \tag{(9b)}$$

Fig. 7. shows the theoretical response-time curve of the comparator derived on this basis. Two curves are shown, the upper giving the uncertainty which occurs when measurement starts during a non-coincidence period. The time delay due to the uncertainty is proportional to phase displacement and has a maximum of T/2 at the operating threshold $\phi = \pi/2$. The operating time is virtually constant for phase shifts of less than 60°. Thereafter, the time is delayed progressively until it becomes infinite at the operating threshold.

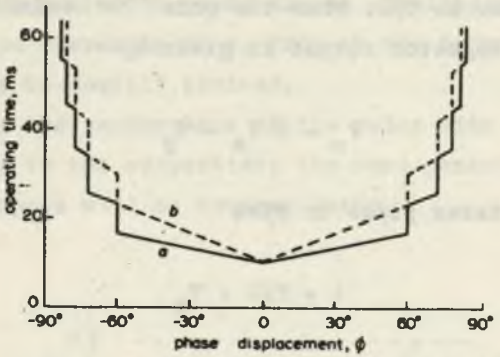

Fig. 7. Operating time as a function of phase displacement
a - minimum timing, b - maximum timing

The virtue of this type of characteristic is that it combines the advantages of very high speed of operation with very accurate measurement at the threshold. This characteristic is a direct consequence of the fact that the design is based on the transient response as discussed earlier. In the authors' view, it is fundamental that, if the transient response is to be satisfactory, a graded response time is an inevitability.

4. Practical considerations

4.1. Relay sensitivity

The inherent dynamic response was derived above on the assumption that the comparator was infinitely sensitive, since it was assumeded that measurement took place during coincidence without regard to amplitude. This is undesirable in practice, since the condition of one, or both, inputs being zero should be a positive restraint condition. This is achieved in practice by arranging that coincidence outputs are only initiated when both input signals simultaneously exceed some minimum value known as the setting, which need not necessarily be the same for the two inputs.

The effect of setting on performance is readily taken into account. It is merely necessary to compute the apparent phase shift as seen by the integrator, this being related to the true phase shift and to the ratio of each signal input to its setting. For example, if the two signals are in phase, the peak value of each should be $\sqrt{2}$ times the setting in order that the apparent phase shift is 90^{o}. This provides the useful criterion that the r.m.s input at the threshold should be equal to the setting. Furthermore, for this in-phase condition, the smallest input signal will determine operation.

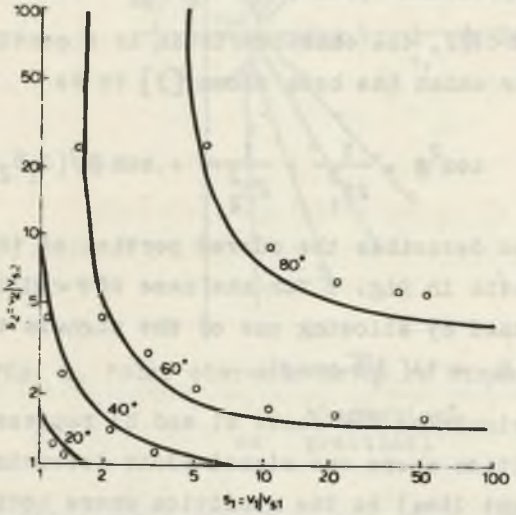

Fig. 8. Constant phase angle curves, degrees indicated between S_1 and S_2

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Fig. 8 shows the relationship between the ratios $S_1 = V_1/V_{s1}$ and $S_2 = V_2/V_{s2}$ with ϕ as a parameter, where V_{s1} and V_{s2} are comparator voltage settings. The salient features of the threshold characteristics are:

a) For $\phi = 0$, the characteristic comprises two intersecting straight lines, $V_1/V_{s1} = 1$ and $V_2/V_{s2} = 1$.

b) For $0 < \phi < \pi/4$, the characteristic is divided into three regions; i.e. a straight line $V_1/V_{s1} = 1$, a continuous curve and a straight line $V_2/V_{s2} = 1$. It has been shown [3] that transition points from the straight lines to the curve are described by the equation

$$V_1/V_{s1} = 1/\{\sqrt{2}\cos(\phi + \pi/4)\} \qquad (10)$$

The same expression applies for V_2/V_{s2} because of the symmetry.

c) For $\pi/4 < \phi < \pi/2$, the characteristic is a continuous curve, the equation for which has been shown [3] to be

$$\cos^2\phi = \frac{1}{2S_1^2} + \frac{1}{2S_2^2} + \sin\phi/(S_1S_2) \qquad (11)$$

Eqn. Il also describes the curved portion of the discontinuous characteristic in Fig. 8 for the case of $\phi < \pi/4$. The asymptotes are determined by allowing one of the signals to approach infinity; e.g. $S_1 = 1/(\sqrt{2}\cos\phi)$.

The discontinuities for cases a) and b) represent the transition from the condition where one signal alone determines the characteristic (straight line) to the condition where both signals determine the characteristic (continuous courve). In particular, these curves are useful for deriving the more familiar polar characteristic a family of which is shown in Fig. 9, drawn for constant values of S_1 so that the curves relate S_2 to ϕ. Again, both theoretical and practical curves are shown and the effect of the comparator setting is evident, where it is shown to produce a discontinuous characteristic made up of straight lines and the arc of a circle with radius $S_2 = 1$ and centre at the origin. The polar curves of Fig. 9, are useful in assessing practical relay performance and application

suitability in a power system; in this context, the features of the directional characteristic are well known.

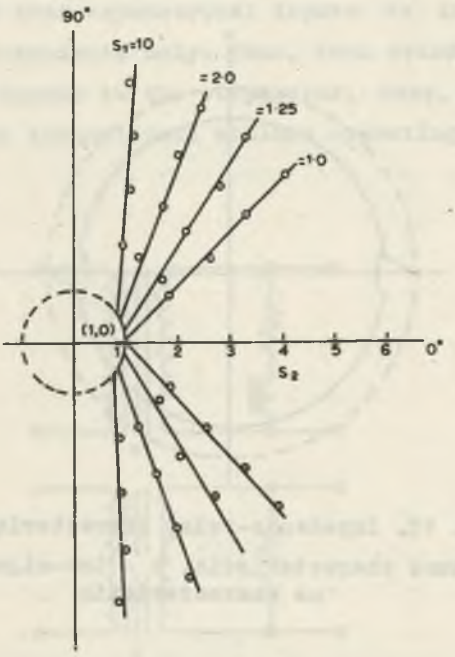

Fig. 9. Polar characteristic of directional relay

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Fig. 10 illustrates the plain impendance characteristic obtained with the same kind of comparator using the appropriate input transformation. This characteristic is drawn using parameters of impedance in the complex plane, the broken line defining the high-level (ideal) characteristic. The full-line characteristic is obtained at lower signal levels; it can be shown that the two semicircular indents reduce in size at more practical input signal levels as the circle expands towards the broken-line characteristic.

The sensitivity attainable using transistors usually reduces such imperfections in characteristics to very small proportions and,

in any case, a fuller analytical treatment is warranted when compensation using nonlinear elements is used.

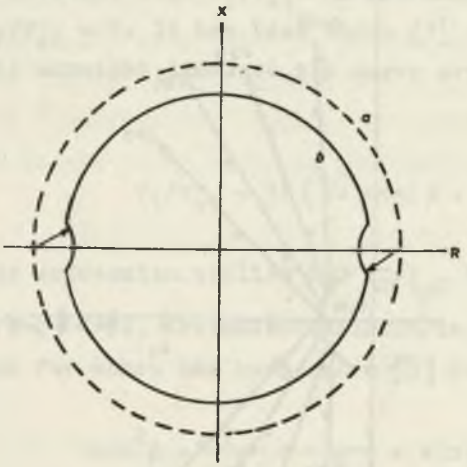

Fig. 10. Impedance-relay characteristic
a - ideal impedance characteristic, b - low-signal-level impedance characteristic

4.2. Practical derivation of the input quantities of a comparator

Inevitably the phase-shifting requirements in the measuring and mixing circuit of Fig. 1 will influence the dynamic performance of the final scheme, and the transient response of this circuit must be carefully assessed even when transient-free comparator circuits are being used. Mimic impedances in the current circuit are generally preferred, and two well known arrangements are illustrated in Figs 11a and b. Under ideal conditions, the true mimic-impedance arrangement of Fig. 11a results in the offset d.c.transient components in the measuring input to the comparator being eliminated. In practice, however, the not unusual mismatch of angle between the mimic and the protected line may result in transient components of the same polarity on both inputs, and for this reason the imper-

fect mimic impedance or transactor of Fig. 11b is preferred. The steady-state responses of the two arrangements in Fig. 11 are identical, but for all practical line angles the transactor is a transient filter, so that asymmetrical inputs to the comparator are due to voltage transients only. Thus, when transient components exist in both inputs to the comparator, they, will be of opposite polarity and the critical minimum operating-time of 10ms

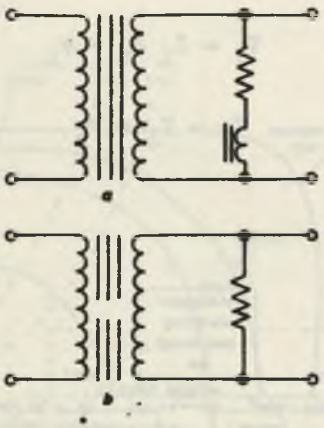

Fig. 11. Alternative mimic impedance arrangements
a - True mimic, b - transformer-reactor

can be preserved. Other practical advantages of the transactor include the fact that only one iron-cored element is required and that the transient flux levels in the core are much less onerous than those encountered in the auxiliary current transformer of Fig. 11a. All these points were fully exploited in the development of the practical prototype relay discussed in Section 5. The practical aspects of design of the measuring circuit include the requirment for good surge proofing, which is conveniently achieved by screening the transactor and voltage transformer units; these units include the necessary means for adjusting the phase-angle and relay impedance settings.

5. Dynamic performance of the practical protype relay

Dynamic testing of a prototype relay was done under controlled conditions on a test bench, one phase of which is shown in schematic form in Fig. 12. The line impedance of this apparatus is variable in magnitude, the X/R ratio being constant: the source impedance is also variable with the X/R ratio being nominally 30 but varying somewhat with the magnitude setting. The characteristics presented here were obtained from the relay arranged to give a polarised-mho characteristic, with the well known vector-mixing relationships:

$$V_1 = I_L Z_R - V_L \tag{14}$$

$$V_2 = V_L + V_p \tag{15}$$

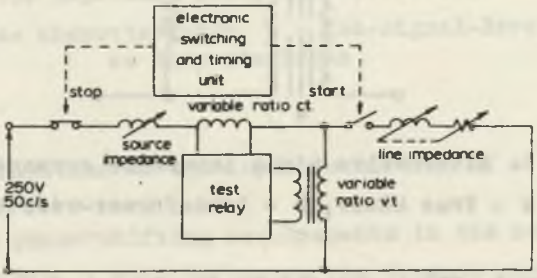

Fig. 12. Single-phase representation of test bench

Characteritics were measured in order to confirm the high speed of operation and inherent accuracy of measurement under transient fault conditions; it was arranged that the minimum operating time of the comparator under test should be 15 ms. Fig. 13 shows relay accuracy plotted against system impedance ratio (s.i.r) with operating time as a parameter and for zero-offset d.c. transient in the primary circuit; this curve therefore describes the performance of both replica impedance and transactor since their steady-state per-

formances are identical. In Fig. 13 accuracy is defined as the ratio

$$x = \frac{Z_L}{Z_R} = \frac{\text{impedance to point of fault}}{\text{impedance setting of relay}}$$

and s.i.r. is defined as

$$y = \frac{Z_S}{Z_R} = \frac{\text{system source impedance}}{\text{impedance setting of relay}}$$

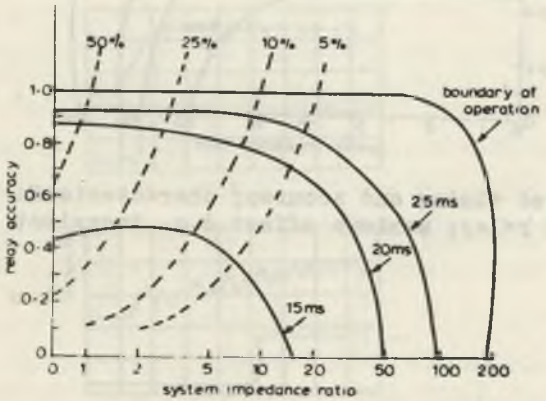

Fig. 13. Measured timing and accuracy characteristic of polarised-mho relay; no offset d.c. transient

———constant-timing contours, - - - constant-voltage contours

Fig. 14. shows the corresponding curves plotted for maximum offset d.c. transient in the primary circuit; comparison of the curves defining the boundary of operation in Figs. 13 and 14 shows there to be no transient overreach and clearly illustrates the transient-free nature of the comparator. Inspection of these curves shows that the variation in operating time is not significant in the two extreme cases. As an alternative, the test results are presented in the form of constant-voltage contours superimposed on the constant-operating-time contours. These are shown as broken-line curves in Fig. 13. When these curves are plotted in the

form of operating time against relay accuracy, as in Fig. 15, the definite-time characteristic is clearly shown; i.e. the characteristic is flat over a high proportion of the line length, even for low operating voltages.

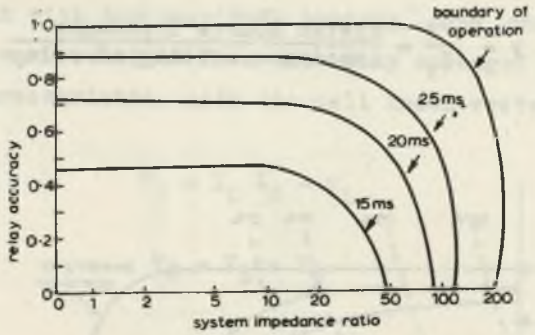

Fig. 14. Measured timing and accuracy characteristic of polarised-mho relay; maximum offset d.c. transient

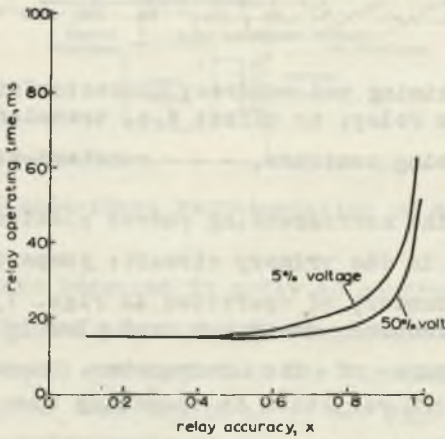

Fig. 15. Polarised-mho constant-voltage contours

Fig. 16 serves to ilustrate dynamic performance in terms of oscillograms of the output waveforms of the integrator and level detector. The waveform at "a" defines the inherent operating time, being for the close-in fault condition. The wavefors at "b" and "c" are for operation 2% inside and outside the operating boundary, respectively. The stability under the onerous test conditions specified is evident, the effects of the alternate wide and narrow pulses driving the integrator during the transient period being apparent.

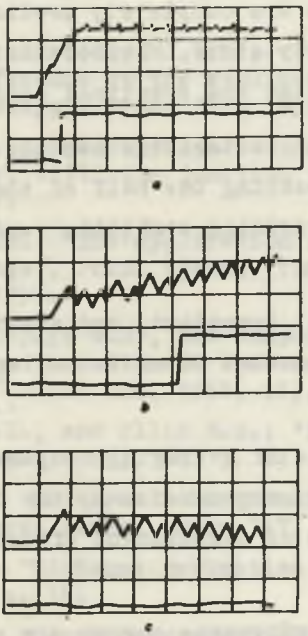

Fig. 16. Practical relay integrator and trip waveforms; s.i.r. y = 10, X/R = 28,6, graticule lines at 20 ms intervals

a) x = 0 b) x = 0.98 c) x = 1.02

6. Conclusions

For comparators based on the principle of block comparison, the generalised analysis given in the Appendix 9 establishes the cor-

responding indentity of output waveform from the basic measuring circuit for a given transformation procedure. Thus, for particular characteristics, block-comparison comparators using either phase or amplitude comparison can be designed to have identical dynamic performance, and the significance of claims purporting to distinguish inherently between them are shown to be unfounded.

The broad general requirements of static relays have been considered, and it is clear that there are a number of firm reasons for using the principle of block-average comparison. The principal reasons are the following:

a) Such relaying systems are completely predictable; desirable transient, and hence steady-state, characteristics can be defined, the equations formulated and practical circuits realised.

b) The controlled time characteristic has the virtue that minimum operating times approaching one half of the system period can be attained without sacrificing stability under marginal conditions.

c) As a consequence of b) transient, and steady-state, operating boundaries coincide so that there is no tendency for transient overreach to occur.

d) Owing to the principle of averaging comparator signals on both half-cycles of the primary waveforms, the degree of primary transient d.c. offset has no significant effect on the speed of operation.

Static and dynamic performance curves are presented in this paper for a practical relay of a type which has seen considerable field service; Figs. 13-16 are in close agreement with the performance originally specified. Further information on the performance of such systems in the field is becoming available, and all results to date justify the confidence resulting from laboratory tests.

7. Acknowledgments

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9. Appendix

Relationship between amplitude and phase comparators

Consider two relay devices indicated in Figs. 17a and b.The one indicated in Fig. 17a is a differential bridge in which

$$S_{out} = |S_a| - |S_b| \text{ instantaneously} \tag{15}$$

The device in Fig. 17b is basically a coincidence circuit and has the following operating law:

$$\left.\begin{aligned}
&\text{a)} \quad S_{out} = +|S_x| \text{ if } |S_x| < |S_y|, \text{ and } S_x/S_y > 0 \\
&\text{b)} \quad S_{out} = -|S_x| \text{ if } |S_x| < |S_y|, \text{ and } S_x/S_y < 0 \\
&\text{c)} \quad S_{out} = +|S_y| \text{ if } |S_x| > |S_y|, \text{ and } S_x/S_y > 0 \\
&\text{d)} \quad S_{out} = -|S_y| \text{ if } |S_x| > |S_y|, \text{ and } S_x/S_y < 0
\end{aligned}\right\} \tag{16}$$

The second device effectively produces an output signal which is equal in magnitude to the smaller of the two input signals, is positive in sign when the input signals have the same polarity, and is negative in the alternative case.

If the following substitution is made in eqn. 15:

$$S_a = (S_x + S_y)/2$$

$$S_b = (S_x - S_y)/2$$

and thus

$$2S_{out} = |S_x + S_y| - |S_x - S_y| \tag{17}$$

then the four cases listed in eqns. 16, a)-d) inclusive need to be considered:

a) $$|S_x| > |S_y| \text{ and } S_x/S_y > 0$$

thus $$2S_{out} = S_x + S_y - (S_x - S_y)$$

and $$S_{out} = S_y$$

b) $$|S_x| > |S_y| \text{ and } S_x/S_y < 0$$

thus $$2S_{out} = S_x - S_y - (S_x + S_y)$$

and $$S_{out} = -S_y$$

c) $$|S_x| < |S_y| \text{ and } S_x/S_y > 0$$

thus $$2S_{out} = S_x + S_y - (S_y - S_x)$$

and $$S_{out} = S_x$$

d) $$|S_x| < |S_y| \text{ and } S_x/S_y < 0$$

thus $$2S_{out} = S_y - S_x - (S_x + S_y)$$

and $$S_{out} = - S_x$$

It can be seen that the operating law of the arrangement in Fig. 17a is the same as that of Fig. 17b under the specified transformation. The transformation is reversible, so that „b" would have the same characteristic as „a" if

$$S_x = S_a + S_b$$

$$S_y = S_a - S_b$$

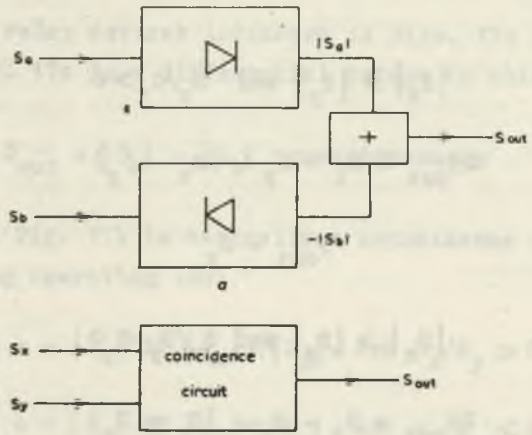

Fig. 17. Theoretical comparator block schematics
a - Amplitude comparator, b - Phase comparator

Since the equivalence is based on instantaneous values, it follows that the result is perfectly general. Consequently, the performance of one device will be identical with that of the other, provided that the output signals are subjected to the same constraints, i.e. amplitude limiting, integration etc.

It is well known that the device of Fig. 17a has a mean output voltage of zero when S_1 and S_2 are sinusoidal voltages of equal amplitude irrespective of phase, while b has a mean output voltage of zero when energised with sinusoidal signals displaced in phase by 90° irrespective of amplitude. It follows that the former principle forms the basis for amplitude comparison; the latter for block phase comparison.

In practice, it is customary to introduce amplitude limiting in a, i.e. the rectifier-bridge moving-coil system, and in b, i.e. the static phase-comparator, as described.

It is possible to repeat the argument for comparators with non-linear operating criteria, e.g. a square-law beam relay, and the-

reby derive the relations for equivalence. It is equally evident that it is not permissible to compare the performance of devices which have nonequivalent laws of operation. This includes ancillary devices such as voltage limiters, integrators and so on. For example, the performance of a rectifier/moving-coil system is modified very considerably by the introduction of voltage limiters.

The important conclusion to be drawn from the analysis here is that, if amplitude and phase-comparators have identical operating laws, there is no need to consider their dynamic characteristics separately; any remarks which apply to one apply to the other. This is particularly the case in this paper where a desired operating principle of signal processing is defined and applies to both comparator principles.

FIGURES DESCRIPTIONS

Fig. 1. Basic block average comparison relay

Fig. 2. Relay waveforms ($\phi > \pi/2$).
a - Input signals to coincidence circuit, b - Output from coincidence circuit (i) - Upper limit, (ii) - Set level, (iii) - Reset level, c - Integrator output

Fig. 3. Relay waveforms ($\phi < \pi/2$)
a - Input signals to coincidence circuit, b - Output from coincidence circuit, (i)-Upper limit, (ii) - Set level , (iii) - Reset level, c - Integrator output

Fig. 4. Realy waveforms for marginal operation ($\phi = \pi/2$)
a - Input signals to coincidence circuit, b - Output from coincidence circuit (i) - Upper limit, (ii) Set level, (iii) Reset level, c - Integrator output

Fig. 5. Relay waveforms with d.c. offset in V_c
a - Input signals to coincidence circuit, b - Output from coincidence circuit, (i) Upper limit, (ii) Set level, (iii) Reset level, c - Integrator output

Fig. 6. Integrator output waveform used to determine operating time

Fig. 7. Operating time as a function of phase displacement
a - minimum timing, b - maximum timing

Fig. 8. Constant phase angle curves; degrees indicated between S_1 and S_2
——— theoretical
oo practical

Fig. 9. Polar characteristic of directional relay
----- theoretical
oo practical

Fig. 10. Impedance-relay characteristic
a - ideal impedance characteristic, b - low-signal-level impedance characteristic

Fig. 11. Alternative mimic impedance arrangements
a - True mimic, b - transformer-reactor

Fig. 12. Single-phase representation of test bench

Fig. 13. Measured timing and accuracy characteristic of polarised-mho relay; no offset d.c. transient
———· constant-timing contours,
-----· constant-voltage contours

Fig. 14. Measured timing and accuracy characteristic of polarised-mho relay; maximum offset d.c. transient

Fig. 15. Polarised-mho constant-voltage contours

Fig. 16. Pratical relay integrator and trip waveforms; s.i.r. y = 10, X/R = 28,6, graticule lines at 20 ms intervals
a) x = 0. b) x = 0,98 c) x = 1.02

Fig. 17. Theoretical comparator block schematics
a - Amplitude comparator, b - phase comparator

ZESZYTY NAUKOWE POLITECHNIKI ŚLĄSKIEJ 1971

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KOMPARATORY STATYCZNE W ZABEZPIECZENIACH ODLEGŁOŚCIOWYCH - KONSTRUKCJA OPTYMALNA ZE WZGLĘDÓW DYNAMICZNYCH

S t r e s z c z e n i e

Przekaźniki z tranzystorowymi komparatorami amplitudy i fazy są z powodzeniem stosowane od roku 1957 i na przestrzeni lat wykazały swoją wyższość nad przekaźnikami o elementach elektromechanicznych. Można konstruować komparatory tranzystorowe o charakterystykach takich jakie posiadają komparatory elektromagnetyczne lub indukcyjne ale można też uzyskać charakterystyki niedostępne dla elementów konwencjonalnych.

Konstrukcje komparatorów amplitudy i fazy mogą być oparte na trzech odmiennych zasadach: porównywania bezpośredniego wartości chwilowych przebiegów, porównywania wartości chwilowych z zastosowaniem następnie członu całkującego do wytworzenia sygnału zadziałania, oraz na zasadzie impulsowej. Najbardziej przydatne z uwagi na swoje własności dynamiczne okazują się komparatory z członami całkującymi.

W artykule zamieszczono dowód tezy, że komparatory amplitudy i fazy oparte na tej samej zasadzie działania wytwarzają identyczne chwilowe sygnały wyjściowe, oczywiście pod warunkiem, że obwody zewnętrzne przetwarzania sygnałów wejściowych są identyczne, podobnie jak obwody przyłączone do wyjść obydwóch komparatorów. Dynamika odpowiednich komparatorów amplitudy i fazy jest więc taka sama, wobec czego autorzy poprzestali na rozpatrywaniu wyłącznie

komparatorów fazy, zwłaszcza, że tranzystory jako takie bardziej nadają się do konstrukcji komparatorów fazy.

W komparatorze fazy z członem całkującym sygnały wejściowe napięciowe przetworzone odpowiednio z napięcia i prądu obciążenia linii dostarczane są do członu pomiarowego koincydencyjnego,który wytwarza impulsy o jednakowej amplitudzie: dodatnie przy jednakowych i ujemnie przy przeciwnych znakach obydwóch napięć. W przeciwieństwie do zwykłego komparatora wartości chwilowych następuje tutaj porównywanie sygnałów wejściowych w obydwóch półokresach,przy czym impulsy będące wynikiem porównania sygnałów wprowadzane są do członu całkującego, na którego wyjściu otrzymuje się sygnał o wartości szczytowej zależnej od szerokości impulsów. Szerokość ta zależy z kolei od czasów trwania zgodności znaków porównywanych napięć czyli od przesunięcia fazowego między nimi. Pobudzenie elementu wyjściowego następuje z chwilą gdy na wyjściu członu całkującego pojawi się sygnał o amplitudzie przekraczającej nastawioną wartość. Zachodzi to w przypadku gdy kąt przesunięcia fazowego pomiędzy obydwoma napięciami jest mniejszy od $\pi/2$. Dla kątów większych od $\pi/2$ człon całkujący wytwarza sygnały o amplitudzie mniejszej od poziomu pobudzenia elementu wyjściowego.

Wyższość komparatorów z członami całkującymi nad komparatorami zwykłymi wartości chwilowych lub komparatorami impulsowymi wynika stąd, że dwa ostatnie, z uwagi na porównywanie wprost wartości chwilowych narażone są na wpływ zakłóceń wywołanych przebiegami przejściowymi. Aby uniknąć fałszywych zadziałań tego rodzaju komparatorów należy zwiększać ich czasy zadziałań lub stosować specjalne układy filtrujące na wejściu. W przypadku komparatorów z członami całkującymi układy takie są zbędne, natomiast czasy zadziałania tych komparatorów mogą być rzędu połowy okresu częstotliwości sieciowej. Nie istnieje niebezpieczeństwo zakłóceń pracy komparatora w wyniku przebiegów przejściowych nawet długotrwałych,dokładność pomiaru pozostaje prawie bez zmian w szerokim zakresie pracy. Na czas zadziałania nie ma istotnego wpływu chwila wystąpienia uszkodzenia w sieci. Komparator z członem całkującym posiada

charakterystykę bardzo zbliżoną do czasowo niezależnej w całym zakresie pracy, z tym, że w pobliżu kąta krytycznego $\pi/2$ czas zadziałania zdąża do nieskończoności.

Dzięki wymienionym zaletom komparatory z członami całkującymi mogą być z powodzeniem stosowane jako elementy członów pomiarowych zabezpieczeń odległościowych. Zalety te znalazły potwierdzenie w wynikach pomiarów jakich dokonano w laboratorium dla komparatora fazy o charakterystyce impedancyjno-kierunkowej (mho). Porównanie charakterystyk dynamicznych tego komparatora przedstawionych jako zależności dokładności pomiaru od impedancji układu dla różnych czasów zadziałania w dwóch różnych przypadkach, a mianowicie:przy ciągłym stałym przebiegu zakłóceniowym oraz w stanie bezzakłóceniowym wskazuje, że zakłócenia nie mają istotnego wpływu na dokładność pomiaru komparatora w szerokim zakresie. Można osiągnąć czasy zadziałania rzędu połowy okresu częstotliwości sieciowej.Charakterystyki statyczne i dynamiczne są określone dla całego zakresu pracy komparatora.

Należy zaznaczyć, że najkrótszy czas zadziałania komparatora z członem całkującym wystąpiłby w przypadku gdyby jeden z porównywanych sygnałów przybrał wartość niezmienną co do znaku w wyniku nałożenia się nań przebiegu zakłóceniowego o charakterze stałym. Zadziałanie komparatora byłoby wówczas fałszywe i należy się od takiego przypadku odstroić przez dobór odpowiedniego minimalnego czasu zadziałania.

Podobnie w przypadku bardzo małych wartości sygnałów wejściowych członu pomiarowego koincydencyjnego nawet przy przesunięciu fazowym równym zero, nie powinno dojść do pojawienia się sygnału wyjściowego tego członu. Odstrojenie się od błędnego zadziałania polega tutaj na dobraniu odpowiednich minimalnych wartości sygnałów wejściowych powodujących zadziałanie członu koincydencyjnego.

OPISY RYSUNKÓW

Rys. 1. Przekaźnik z komparatorem z członem całkującym V_L - napięcie międzyfazowe, I_L - prąd obciążenia, V_1,V_2 - sygnały wejściowe 2 wejściowego komparatora; measuring and mixing circuits - człon rozruchowy; coincidence circuit - człon koincydencyjny (pomiarowy); linear integrator - człon całkujący liniowy; level detector - element wyjściowy (wyłączający); trip - wyłączenie

Rys. 2. Przebiegi czasowe sygnałów członów przekaźnika (przesunięcie fazowe pomiędzy V_1 i $V_2 \phi > \frac{\pi}{2}$.

a) Sygnały wejściowe członu koincydencyjnego (pomiarowego), b) Przebieg wyjściowy członu koincydencyjnego (pomiarowego), (i) Górny poziom, (ii) Wartość nastawiona, (iii) Wartość powrotu, c) Przebieg wyjściowy członu całkującego

Rys. 3. Przebiegi czasowe sygnałów członów przekaźnika (przesunięcie fazowe pomiędzy V_1 i V_2 $\phi < \frac{\pi}{2}$).

Pozostałe opisy te same co pod rys. 2. relay operation - zadziałanie przekaźnika

Rys. 4. Przebiegi czasowe sygnałów członów przekaźnika dla wartości krytycznej kąta przesunięcia fazowego pomiędzy V_1 i V_2 $\phi = \pi/2$
Pozostałe opisy te same co pod rys. 3.

Rys. 5. Przebiegi czasowe sygnałów członów przekaźnika przy zakłóceniu o charakterze stałym w sygnale wejściowym V_2.
Pozostałe opisy te same co pod rys. 3.

Rys. 6. Określenie czasu zadziałania na podstawie przebiegu wyjściowego członu całkującego
Integrator output voltage - napięcie wyjściowe członu całkującego, time, ms - czas, ms, V_s - nastawiona wartość napięcia członu wyjściowego, V_x, V_y - wartości napięć członu wyjściowego odpowiadające przedziałom czasowym T_x i T_y

Rys. 7. Czas zadziałania jako funkcja przesunięcia fazowego; operating time, ms - czas zadziałania, ms; phase displacement, ϕ - przesunięcie fazowe, a) czasy minimalne, b) czasy maksymalne

Rys. 8. Krzywe stałego kąta fazowego; kąt między sygnałami S1 i S2 V_{s1}, V_{s2} - nastawienia napięciowe członu wyjściowego, V_1, V_2 - sygnały wejściowe 2-wejściowego komparatora, S_1, S_2 - wartości względne wejść 1 i 2 (odniesione do nastawień V_1 i V_2), ——— - krzywa teoretyczna
o ooo - krzywa rzeczywista

Rys. 9. Charakterystyka biegunowa przekaźnika kierunkowego
——— - teoretyczna
o o o - rzeczywista
S_1, S_2 - wartości względne wejść 1 i 2 (odniesione do nastawień V_1 i V_2)

Rys. 10. Charakterystyka przekaźnika impedancyjnego
a - Idealna charakterystyka impedancyjna, b - Charakterystyka impedancyjna przy niskim poziomie sygnału

Rys. 11. Alternatywne układy impedancji wyrównawczych
a - wyrównanie dokładne, b - transformator - dławik

Rys. 12. Stanowisko pomiarowe-połączenia dla jednej fazy; electronic switching and timing unit - układ elektroniczny włączający i mierzący czas
variable ratio c.t. - przekładnik prądowy o zmiennej przekładni, variable ratio v.t. - przekładnik napięciowy o zmiennej przekładni, Source impedance - impedancja źródła, line impedance - impedancja linii, test relay - badany przekaźnik.

Rys. 13. Rzeczywiste charakterystyki zmierzone czasów zadziałania i dokładności przekaźnika spolaryzowanego impedancyjno-kierunkowego (mho); bez przebiegów zakłóceniowych przejściowych o charakterze stałym, relay accuracy - dokładność przekaźnika, system impedance ratio - stosunek impedancji źródła systemu do wartości impedancji nastawionej na przekaźniku, boundary of operation - granica działania
——— krzywe stałego czasu
- - - - krzywe stałego napięcia

Rys. 14. Rzeczywiste charakterystyki zmierzone czasów zadziałania i dokładności przekaźnika spolaryzowanego impedancyjno-kierunkowego (mho) przy maksymalnym zakłóceniowym przebiegu przejściowym o charakterze stałym.
realy accuracy - dokładność przekaźnika, system impedance ratio - stosunek impedancji systemu do wartości impedancji nastawionej na przekaźniku, boundary of operation - granica działania

Rys. 15. Krzywe stałego napięcia dla spolaryzowanego przekaźnika impedancyjno-kierunkowego (mho)
relay operating time, ms - czas zadziałania przekaźnika, ms, relay accuracy - dokładność przekaźnika, voltage - napięcie

Rys. 16. Przebiegi całkowania i wyłączenia dla badanego przekaźnika
s.i.r - stosunek impedancji źródła systemu do wartości impedancji nastawionej na przekaźniku, graticule lines at 20 ms intervals - linie skali czasu w odstępach 20 ms

Rys. 17. Teoretyczne schematy blokowe komparatorów
a - Komparator amplitudy, b - Komparator fazy, S_{out} - sygnał wyjściowy, coincidence circuit - człon koincydencyjny (pomiarowy).

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СТАТИЧЕСКИЕ КОМПАРАТОРЫ, ПРИМЕНЯЕМЫЕ В ДИСТАНЦИОННЫХ ЗАЩИТАХ - ОПТИМАЛЬНАЯ КОНСТРУКЦИЯ, ВОЗНИКАЮЩАЯ ИЗ ДИНАМИЧЕСКИХ УСЛОВИЙ

К о р о т к о е с о д е р ж а н и е

Реле с амплитудными и фазными транзисторными компараторами с успехом применяются с 1957 г. и на протяжении этих лет показали свои преимущества по сравнению с электромеханическими реле. Существует возможность изготовления транзисторных компараторов имеющих характеристики сходные с характеристиками электромагнитных или индукционных компараторов, но можно тоже получить характеристики недоступные для конвенциональных элементов.

Конструкции амплитудных и фазных компараторов могут быть основаны на трех различных принципах: непосредственного сравнения мгновенных значений процессов, сравнения мгновенных значений с применением интегрирующего элемента для получения исполнительного сигнала, а также на импульсном принципе. Наиболее пригодные, учитывая динамические свойства, оказываются компараторы с интегрирующими элементами.

В статье приведено доказательство тезиса, что амплитудные и фазные компараторы основаны на том же принципе действия, создают идентичные мгновенные входные сигналы, ко-

нечно при условии, что внешние цепи преобразования входных сигналов идентичны и цепи включенные на выходе этих компараторов - сходны.

Динамика соответственных амплитудных и фазных компараторов оказывается одинаковой в связи с чем авторы ограничиваются рассмотрением исключительно фазных компараторов главным образом потому, что транзисторы как таковые более пригодны для конструкции фазных компараторов.

В фазном компараторе с интегрирующим элементом входные сигналы напряжения, получаемые в результате соответственного преобразования напряжения и тока нагрузки линии подаются на вход совпадающего измерительного элемента, создающий импульсы одинаковой амплитуды: положительные при одинаковых и отрицательные при противоположных знаках обоих напряжений.

В противоположность к обыкновенному компаратору мгновенных значений здесь происходит сравнение сигналов в обоих полупериодах, при чем импульсы, получаемые в результате сравнения сигналов, передаются на интегрирующий элемент на выходе которого создается сигнал, максимальное значение которого зависит от ширины импульсов. Ширина эта, в свою очередь, зависит от продолжительности соответствия знаков сравниваемых напряжений, т.е. от сдвига фаз между ними. Пуск выходного элемента происходит в момент, когда на выходе интегрирующего элемента появляется сигнал с амплитудой превышающей установленное значение. Происходит это в случае, когда угол сдвига фаз между двумя напряжениями меньше $\pi/2$. Для углов больше $\pi/2$ интегрирующий элемент создает сигналы с амплитудой ниже уровня пуска выходного элемента.

Преимущества компараторов с интегрирующими элементами перед обыкновенными компараторами мгновенных значений или импульсными компараторами состоят в том, что два последних, в виду непосредственного сравнивания мгновенных зна-

чений подвергнуты влиянию помех, возникающих от переходных процессов. Во избежании ложных действий этого рода компараторов следует увеличивать время их действия или применять на выходе специальные системы фильтров. В случае компараторов с интегрирующими элементами эти системы фильтров излишны, но время действия может быть порядка полсвины периода промышленной частоты. Отсутствует опасность помех в работе компаратора в результате переходных процессов даже длительных; точность измерения остается почти без изменений в широком диапазоне работы. На время действия не имеет существенного влияния момент возникновения повреждения в сети. Компаратор с интегрирующим элементом имеет характеристику очень приближенную к временно независимой характеристике в полном диапазоне работы, с тем, что в близи критического угла $\pi/2$ время действия стремится к бесконечности.

Благодаря упомянутым преимуществам компараторы с интегрирующими элементами могут с успехом применяться в качестве измерительных элементов дистанционных защит. Преимущества нашли подтверждение в результатах лабораторных испытаний компаратора фазы, имеющего импедансно-направленную характеристику. Сравнение динамических характеристик этого компаратора, представленных как зависимость точности измерения от импеданса системы для различных времен действия в двух отдельных случаях, а именно: при длительном наличьи помех и в состоянии без помех, показывает что помехи не имеют существенного влияния на точность измерения компаратора в широком диапазоне. Можно добиться времени действия порядка половины периода промышленной частоты.

Статические и динамические характеристики определены для всей области работы компаратора.

Необходимо отметить, что самое короткое время действия компаратора с интегрирующим элементом может выступить в

случае, когда один из сравниваемых сигналов получить постоянное по знаку значение в результате наложения сигнала помехи с постоянном характере процесса. Действие компаратора будет тогда ошибочным и следует отстроиться от таких случаев подбором соответствующего минимального времени действия.

Аналогично, в случае очень малых значений сигналов на входе совпадающего измерительного элемента даже при нулевом сдвиге фаз, не должно быть сигнала на входе этого элемента. Отстройка от ложных действий состоит, в этом случае, на подборе соответствующих минимальных значений входных сигналов, возбуждающих совпадающий измерительный элемент.

ОПИСАНИЕ РИСУНКОВ

Рис. 1. Реле с компаратором с интегрирующим элементом

V_L – линейное напряжение

I_L – ток нагрузки

V_1, V_2 – входные сигналы 2-входного компаратора

measuring and mixing circuits – пусковой элемент
coincidence circuit – совпадающий элемент
linear integrator – линейный интегрирующий член
level detector – выходной (исполнительный) элемент
trip – отключение

Рис. 2. Временные диаграммы сигналов элементов реле фазовой сдвиг между V_1 и V_2 $\phi > \frac{\pi}{2}$)

а) Входные сигналы коинциденционного (измерительного) элемента

б) Выходной пробег коинциденционного (измерительного) элемента

(i) верхний уровень
(ii) значение уставки
(iii) значение возврата

в) Процесс выхода интегрирующего элемента.

Рис. 3. Временные диаграммы сигналов элементов реле (фазовый сдвиг между V_1 и V_2 $\phi < \frac{\pi}{2}$)

Остальные списания как для рис. 2.
relay operation - срабатывание реле

Рис. 4. Временные диаграммы сигналов элементов реле для критических значений угла сдвига фаз между V_1 и V_2 $\phi = \pi/2$.

Остальные описания как для рис. 3.

Рис. 5. Временные диаграммы сигналов элементов реле при наличии во входном сигналв V_2 помехи, имеющей постоянный характер.
Остальные списания как для рис. 3.

Рис. 6. Определение времени декствия на оснсвании процесса выхода интегрирующего элемента

integrator output woltage - выходное напряжение интегрирующего элемента
time, ms - время мсек
V_s - уставка напряжения выходного элемента
V_x, V_y - значения напряжений выходного элемента соответствующие интервалами времени T_x и T_y

Рис. 7. Время действия как функция фазового сдвига

operating time, ms - время действия, сек
phase displacement ϕ - фазовый сдвиг

а) максимальные времена
б) минимальные времена

Рис. 8. Кривые постоянного фазового угла; угол между сигналами S1 и S2

V_{s1}, V_{s2} - уставки напряжений выходного элемента
V_1, V_2 - входные сигналы двуходного компаратсра
S_1, S_2 - относительные значения входов 1 и 2 (отнесенные к уставкам V_1 и V_2)
——— - теоретическая кривая
o o o - действительная кривая

Рис. 9. Полюсная характеристика направленного реле

——— - теоретическая
o o o - действительная
S_1, S_2 - относительные значения входов 1 и 2 (отнесенные к уставкам V_1 и V_2)

Рис. 10. Характеристика импедансного реле

а) идеальная импедансная характеристика
б) импедансная характеристика при низком уровне сигнала

Рис. 11. Альтернативные системы уравнительных импедансов

а) точное уравнивание
б) трансформатор - реактор

Рис. 12. Измерительный стенд - соединение для одной фазы

electronic switching and fiming unit - электронная система включения и измерения времени
variable ratio c.t. - трансформатор с тока изменяющимся коэффициентом трансформации
variable ratio v.t. - трансформатор напряжения с изменяющимся коэффициентом трансформации
Source impedance - импеданс источника
line impedance - импеданс линии
test relay - испытываемое реле

Рис. 13. Действительные измеренные характеристики времен действия и точности поляризованного импедансно-направленного реле (mho); без наличия переходного процесса помех постоянного характера)

relax accuracy - точность реле
system impedance ratio - отношение импеданса системы к значению импеданса уставки реле
boundary of operation - предел действия

——— кривые постоянного времени

------ кривые постоянного напряжения

Рис. 14. Действительные характеристики измеренных времен действия и точиости поляризованного импедансно-направленного реле (mho) при максимальном переходном процессе помех постоянного характера

relay accuracy - точность реле
system impedance ratio - отношение импеданса системы к значению импеданса уставки реле
boundary of operation - предел действия

Рис. 15. Кривые постоянного напряжения для поляризованного импедансно-направленного реле (mho)

relay operating time, ms - время действия реле, мсек
relay accuracy - точность реле
voltage - напряжение

Рис. 16. Процесс интегрирования и отключения испытываемого реле s.i.r. - отношение импеданса системы к значению импеданса уставки реле

graticule lines at 20 ms intervale - деления шкалы времени в интервалах 20 мсек

Рис. 17. Теоретические блок-схемы компараторов

а) Амплитудный компаратор
б) Фазный компаратор

sout - выходный сигнал
coincidence circuit - коинциденционный элемент (измерительный)