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AUTOMATIC SELECTION CHECK
OF A MAGNETIC CORE MEMORY

by Jerzy DAŃDA

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An automatic error detecting system for a linear
selection memory is described. The system checks
decoding operations of memory addressing circuits.
The idea involved is to encode the one-out-of-M
code used on core array inputs back to the binary
code. The latter and the original binary code fed
on address inputs are compared and discrepancies
detected. Reliable components used in the encoder,
being part of the checking system, ensure the ma-
jority of detected errors to be true errors of the
addressing circuits.

The subject of the paper is an automatic check of addressing
circuitry of a linear selection memory.

The a d d r e s s i n g c i r c u i t r y is this part
of the memory which selects memory locations transforming signals
fed to the address inputs and driving core array by word current-
pulses of proper amplitude and timing.

The c o r e a r r a y of linear selection memory is a
rectangular core matrix with M rows and N columns. Rows corre-
spond to memory locations /words/ and columns - to positions /bits/
of words.

In the majority of memories the address of each memory location
is determined by a binary code fed to the memory by signals appear-
ing on K address inputs. This enables the selection of one-out-

of-M locations. Usually, for the economy of the decoding elements such a M is chosen that

$$M = 2^K$$

is satisfied by natural K's.

The operation of the addressing circuitry /mostly consisting of address register, decoding matrices, amplifiers, selection elements and current drivers should be considered from two points of view[*]

1. information processing or performed logic operations which may be described adequately in terms of boolean expressions;

2. signal processing where such operations as amplification, pulse stretching, pulse reshaping etc. are involved.

Concerning point 1, addressing circuits convert the binary code used on address inputs into the one-out-of-M code, used on the core array inputs.

Concerning point 2, addressing circuits transform the signals on address inputs from the standard form into that of word-drive current-pulses with the amplitudes and timing needed to switchover magnetic cores.

In order to increase the reliability of the memory by means of an automatic selection check both information and signal processing should be checked.

The reliability of the checking circuitry should be significantly greater than that of the checked circuitry, in order to obtain a negligible number of checking circuitry errors.

The check of the correctness of code transformation being the main technical problem, may be realized at least by two methods /I,II/. Although they may be reduced to a more general way, they are worth being considered separately.

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[*] As regards p.1 and 2 it is worth while to emphasize that the signal processing in the memory circuitry predominates over the signal processing in other units /such as arithmetic and control units/, where the information standard representation in principle does not change during all logic operations.

Method I consists in converting the one-out-of-M code used on the array inputs back to the binary code by means of an appropriate encoder, and comparing it with the original code on address inputs. This is achieved by a parallel comparator included in the checking circuitry /refer to fig.1/.
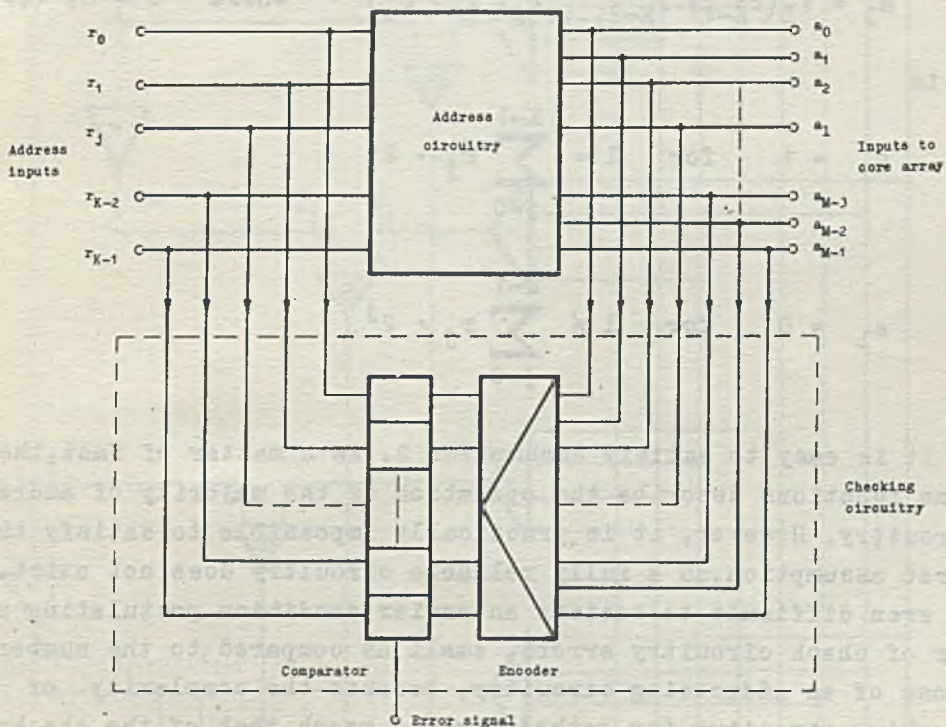

Fig. 1. Check circuitry /Method I/

This method enables us to detect any error which may appear in the addressing circuitry, consisting in:

- lack of pulse on whichever of the outputs a_0, a_1 ... a_{M-1},
- simultaneous appearing of pulses on 2, 3, ..., M outputs,
- lack of pulse on the selected output, and appearing of pulses on 1, 2, 3, ..., M-1 outputs.

This however, requires the following assumptions to be satisfied:

1. The check circuitry built as in fig. 2 is fully errorless.

2. Outputs a_l of the addressing circuitry are described as below by M functions of r_j inputs:

$$a_l = f_l\left(r_{K-1}, r_{K-2},\ldots r_j, r_1, r_0\right) \qquad \text{where} \qquad l = 0, 1,\ldots M-1$$

is

$$a_l = 1 \qquad \text{for} \qquad l = \sum_{j=0}^{K-1} r_j \cdot 2^j$$

$$a_l = 0 \qquad \text{for} \qquad l \ne \sum_{j=0}^{K-1} r_j \cdot 2^j$$

It is easy to satisfy assumption 2. As a matter of fact, the very same functions describe the operation of the majority of addressing circuitry. However, it is practically impossible to satisfy the first assumption, as a fully reliable circuitry does not exist. It is even difficult to satisfy an easier condition postulating a number of check circuitry errors, small as compared to the number of those of an addressing circuitry, because the complexity of the checking circuitry for method I would reach that of the checked circuitry.

The check circuitry of this type /refer to fig. 2/ consists of K NOT elements /'N'/ which supply the variable $\bar{r}_j$, 2K EXCLUSIVE-OR elements /'⊕'/, and 2 K OR-GATES /'+'/ each having $\frac{M-1}{2}$ inputs. OR-GATES form the encoder.

The error signal appears on the output of the OR-GATE, the arguments of which are outputs of EXCLUSIVE-OR elements.

According to the logic diagram /fig. 2/ the error signal b_j for j-th binary position of the address is the following

$$b_j = \left(r_j \oplus c_j\right) + \left(\bar{r}_j \oplus \bar{c}_j\right).$$

$$c_j = \sum_{n=0}^{2^{j}-1} \sum_{m=0}^{M \cdot 2^{-(j+1)}-1} a_{m \cdot 2^{j+1} + n + 2^{j}}$$

Error signal

$$\bar{c}_j = \sum_{n=0}^{2^{j}-1} \sum_{m=0}^{M \cdot 2^{-(j+1)}-1} a_{m \cdot 2^{j+1} + n}$$
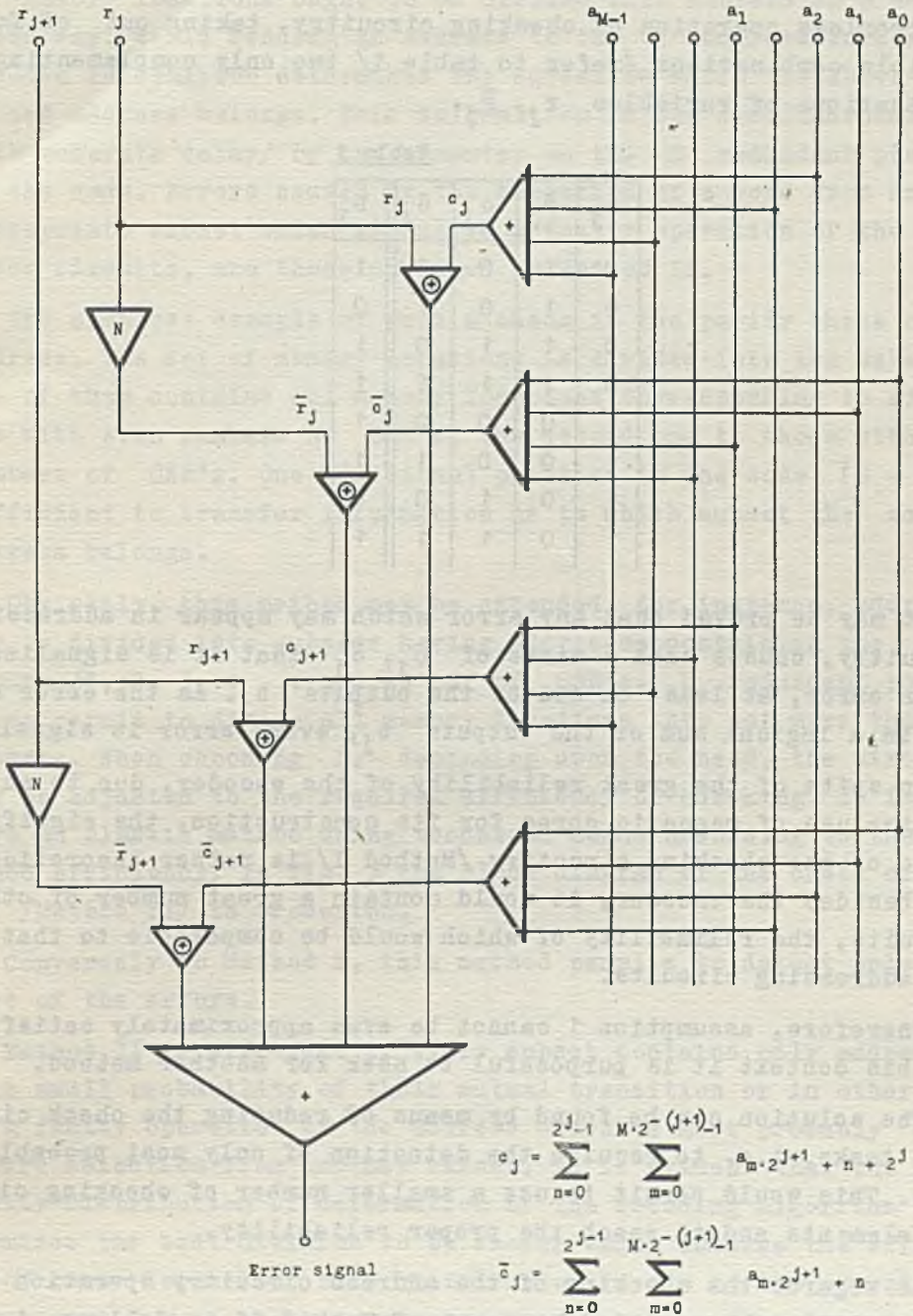
Fig. 2. The fragment of check circuitry logic diagram

It is worth while to notice that use has been made of assumption
on errorless operation of checking circuitry, taking out of four
possible combinations /refer to table 1/ two only complementing
combinations of variables r_j, $\bar{r}_j$.

Table 1

r_j	$\bar{r}_j$	o_j	$\bar{o}_j$	b_j
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1

It may be proved that any error which may appear in addressing
circuitry, causes such a state of c_j, $\bar{c}_j$ that it is signalized
as an error, at least on one of the outputs b_j. As the error sig-
nal is a logical sum of the outputs b_j, every error is signalized.

In spite of the great reliability of the encoder, due to an ex-
tensive use of magnetic cores for its construction, the signifi-
cance of the checking circuitry /Method I/ is rather theoretical,
as, besides the encoder, it would contain a great number of other
circuits, the reliability of which would be comparable to that of
the addressing circuits.

Therefore, assumption 1 cannot be even approximately satisfied.
In this context it is purposeful to seek for another method.

The solution can be found by means of reducing the check circuit-
ry tasks, i.e. to require the detection of only most probable er-
rors. This would permit to use a smaller number of checking circuit-
ry elements and to reach the proper reliability.

As regards the checking of the address circuitry operation this
principle can be realized by means of Method II as follows. A re-
dundant code is to be used on the address inputs. The set of all

2^K memory locations ought to be divided into subsets in a deter-
mined way. While sending an address to the K address inputs, the
encoded information determines the subset to which the above men-
tioned address belongs. This information is fed simultaneously /or
with moderate delay/ by the computer on the D redundant positions
of the code. Errors caused by the selection of a word from an in-
appropriate subset which is due to a faulty operation of the ad-
dress circuits, are those detected by Method II.

The simplest example of such a check is the parity check of the
address. The set of memory locations is divided into two subsets.
One of them contains all memory locations corresponding to addres-
ses with even numbers of ONE's, the second one to those with odd
numbers of ONE's. One additional position in the code $(D = 1)$ is
sufficient to transfer information as to which subset the actual
address belongs.

Obviously, this method may be extended, for instance, addresses
may be divided into subsets having addresses containing the same
amount /1, 2, 3, 4 ... and so on/ of ONE's. D redundant posi-
tions permit to divide all memory locations into not more than 2^D
subsets. When choosing D, depending upon the need, the circuitry
may be adjusted to the required efficiency of checking. It is there-
fore an elastic method using technical means according to the as-
sumed efficiency. In fig. 3 the block diagram of the check circuit-
ry /Method II/ is presented.

Conversely to Method I, this method permits to detect only a
part of the errors.

Method II is efficient if every subset contains only addresses
with small probability of their mutual transition or in other words
if a faulty operation of the address circuits most probably cause
a word selection from another subset. It is evident that the proba-
bility distribution of deformation of the decoding algorithm de-
termines the best division to be chosen which ensures the efficien-
cy of error detection. This distribution is due to the operating
experience, or it may be evaluated on the basis of qualitative ana-
lysis of the circuits. An effective encoding of information on the
address assignment to a subset is chiefly possible only if the num-

ber of error types is small. On the other hand it is worth while
emphasizing that the constructor may somehow influence the probabi-
lity distribution of the types of errors, for instance by changing
the dividing of circuits in the plug-in units. This is the case
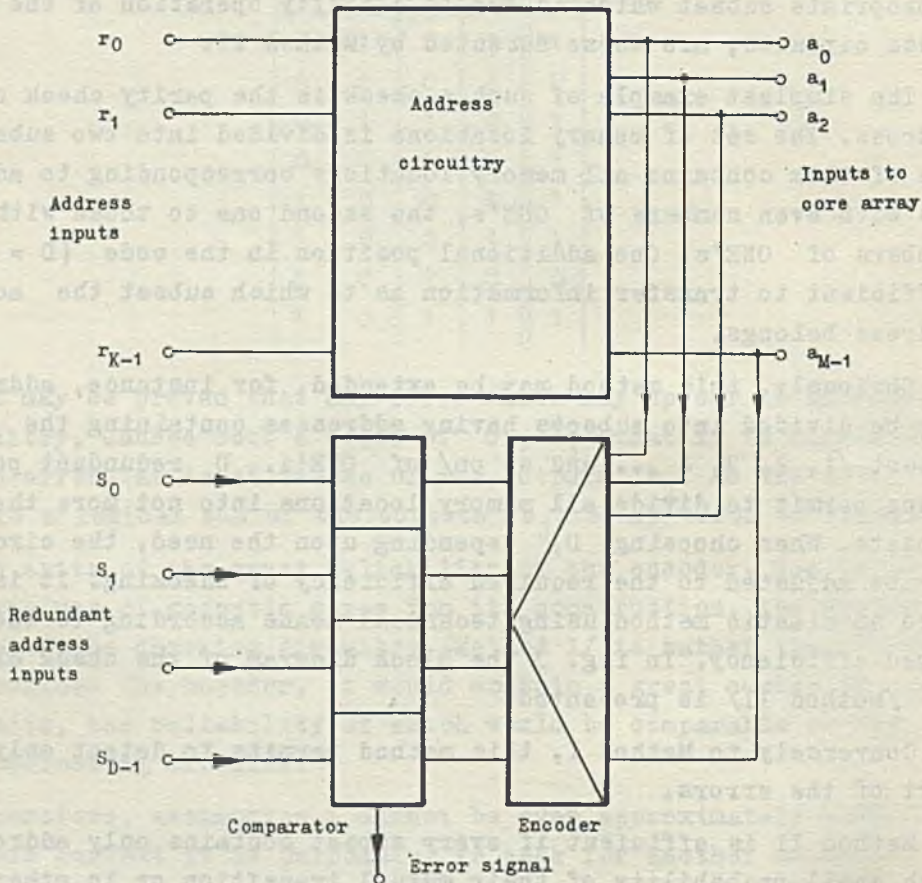when intermittent errors caused by connectors are a problem.

Fig. 3. Block diagram of check circuitry /Method II/.

Summarizing, the construction of the checked circuitry and that
of the checking circuitry should mutually influence one another,
this resulting in a system the errors of which are easy to be de-
tected.

An essential constructional problem appearing in both checking circuits /Method I and II/ is to build reliable multiargument or-gates /of several hundred arguments/. A great amount of arguments and the current-source signals on the inputs of or-gates disquali-fy the most popular diode realization. The solution which satisfies both requirements very well,uses non-linearity of rectangular his-teresis loop cores. This consists in adjoining one additional core to each word line. While selecting a word line, the additional core is switched over and output pulses induced in reading wires. Each or-gate is made by one separate reading wire. Each reading wire is threaded only through additional cores of these word lines which are arguments of the very or-gate. A reading amplifier connected to each wire, amplifies and standarizes signals. The circuit diag-ram of the solution is shown in fig. 4. In fig. 5 a fragment of the encoder plate used in the PAO 4096/28 memory [3] is presented. Referring to fig. 5 there are only two reading wires as in the me-mory the II-nd method II of the check has been applied in its sim-plest version, performing the parity check. Contacts visible in the bottom part of fig. 5 serve to check the word-line current by means of voltage measurement on the inserted resistance /0,3 Ω/. They are used because of the prototype character of the memory.
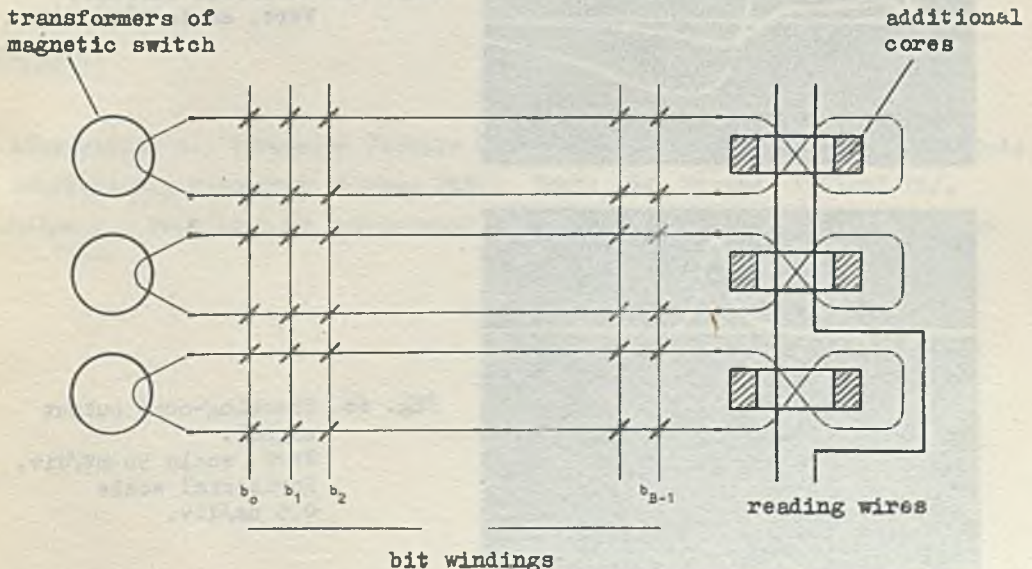

Fig. 4. Circuit diagram of a part of the checking circuitry /with magnetic cores/.
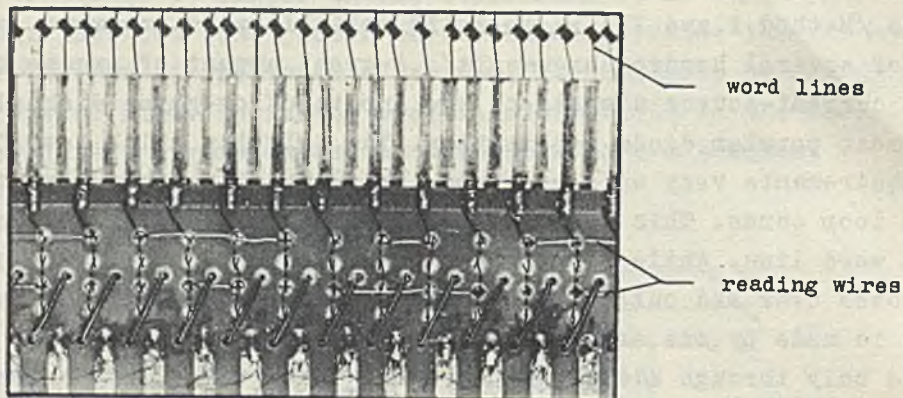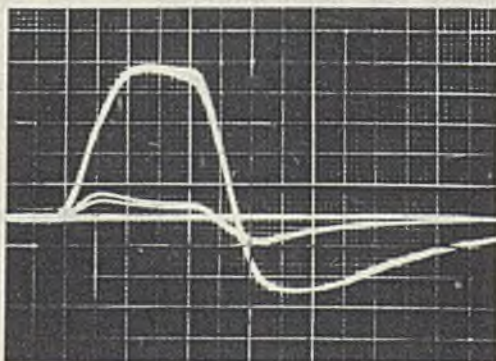
Fig. 5. The fragment of the encoder plate.

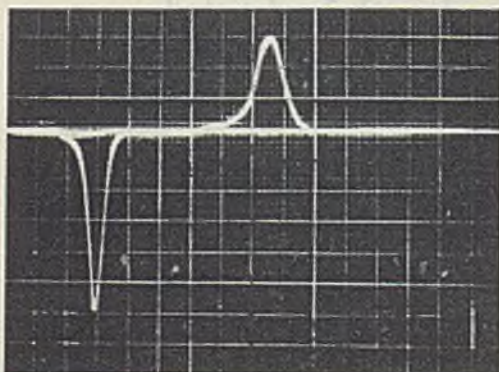Fig. 6a. Word-line current.
         Vert. scale 100 mA/div.

Fig. 6b. Checking-core output
         signal.
         Vert. scale 50 mV/div.
         Horizontal scale
         0,5 µs/div.

The current waveform in the word-line is shown in the oscillo-
gram, fig. 6a, which was done by means of a four-fold superimposing
of current pulses, twice for a full-selected word line and twice
when the magnetic-switch core driving the word line was half select-
ed. A great uniformity of the current waveforms as well as a good
selection ratio are quite evident. Fig. 6b presents the voltage re-
sponse of the checking core in the full-selected line.

It is worth noticing that the construction of a multiargument
or-gate used in a check circuitry may also be used to realize per-
manent storage combined with a working memory. One more additional
core should be placed in each word line for this purpose. Each read-
ing wire representing one binary position of the word is threaded
only through those cores where ONE's are to be stored.

Such a solution is very similar to the construction of the per-
manent storage PAS-2 described in [1] and [2]. It has the virtue
of using the address circuits of the working memory. The reading
amplifiers are the only additional equipment. Moreover, the trouble-
some procedure of noise compensation from half-selected cores might
be omitted because of the linear selection applied instead of the
coincident-current selection.

References

1. ŁUKASZEWICZ L.: Permanent Ferrite Core Storage, Prace ZAM, Warsaw 1960:A4.
2. BOLIŃSKI R.: Permanent storage PAS-2, Prace IMM, Warsaw 1963:B2/15/.
3. DANDA J.: Ferrite Core Operational Memory, Report IMM, T-OP-27-D, Warsaw
      1963.

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