PRACE Instytutu Maszyn Matematycznych PAN

Praca A 5 (22)

ON THE RECOGNITION OF ASYNCHRONOUS PARALLEL ADDER COMPLETION

by Stanisław MAJERSKI

P R A C E

Instytutu Maszyn Matematycznych

T. II Praca A 5/22/

ON THE RECOGNITION OF ASYNCHRONOUS PARALLEL ADDER COMPLETION

by Stanisław MAJERSKI

Warszawa 1965

Instytut Maszyn Matematycznych
Praca A 5/22/

681.14-523.8:621.374

ON THE RECOGNITION OF ASYNCHRONOUS PARALLEL ADDER COMPLETION

by Stanisław MAJERSKI

Received February 25th, 1964

The recognition of the completion of electric processes is a very important problem in many digital circuits. This mainly concerns adders, for which the recognition of the operation completion decisively influences the speed of computations performed in a computer. The paper presents three methods of the recognition of asynchronous parallel adder completion. Namely, the blocking method, being some modification of the known methods of the recognition of adder completion, the delay lines method, and the method of differentiators. Some imperfections of some existing methods are indicated and ways are suggested to avoid them. Notes on conditions that should be satisfied by correct solutions are provided.

1. INTRODUCTION

The operation speed of a determined digital circuit constructed in static technique is subject to great fluctuations and it depends on the kind of information that is being processed in the circuit, on the changes of electric parameters of the circuit elements, on the changes of the supply voltages and air conditions. In particular for parallel adders constructed in static technique, the time of performance of a determined operation /for instance addition/ fluctuates in large limits and depends upon the operation arguments. The maximal operation time of the adder is often many times greater than the mean value of the time. This is the reason for the purposefulness of using such adder solutions which

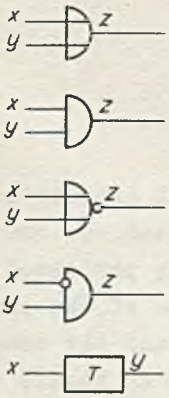
enable the recognition of the completion of electric processes during a determined operation performed in the adder.

The problem of the recognition of a parallel binary adder completion has been dealt with in papers [1], [2], [3], [4], [5], [6], [7]. However, in the author's opinion, some of these solutions are not fully correct, in some others the applied circuits are overdeveloped.

The present paper offers some methods of recognition of parallel binary adder completion. These methods are free from the above mentioned imperfections. In order to illustrate the presented methods they were applied to modify the circuits described in papers [4], [2], [3], [5]. The purpose of these modifications was to ensure the correct circuit operation, and, respectively, to simplify the correctly operating circuits.

2. DEFINITIONS AND DENOTATIONS

1. Scheme denotations will be applied as in fig. 1.



or-gate $z = x + y$

and-gate $z = xy$

function-gate for $z = \overline{x+y}$. *The horizontal line denotes negation in the formula.*

function-gate for $z = \bar{x}y$

the delay line delaying by the time T. The relation $x(t) = y(t+T)$ *is obligatory, i.e. state x at the moment t equals state y at the moment* $t+T$

Fig. 1. Scheme denotations used in the paper.

Literal denotations, for instance x, y, z in fig. 1 are used to denote scheme points as well as zero-one states of these points. Literal denotations of gates coincide with denotations of their outputs.

2. We assume two voltage levels corresponding to states 0, 1 and the changes of voltage levels occuring exclusively by steps /all pulses are rectangular/.

3. The delay time of the voltage step on the gate output in relation to that on its input will be called gate propagation time. For a concrete gate this time may be different for a positive and negative voltage step and, moreover, may depend on the kind of gate input on which this step occurs. We assume, that in every case the propagation time τ of each gate satisfies the condition

$$0 < \tau \leqslant \tau_{max} \qquad /1/$$

where the value τ_{max} is fixed for a determined digital technique. In the case when different propagation times are not needed to be distinguished for the given gate k of the cirouit i, its propagation time will be denoted by τ^i_k. If propagation times for a positive and negative voltage step /on the gate output/ must be distinguished, we shall write τ^i_{+k} and τ^i_{-k}. Other cases of distinguishing propagation times will not be discussed in the present paper.

The acceptance of step /rectangular/ voltage changes leads in consequence to an arithmetic addition of propagation times of gates connected in series. The sum of propagation times of these gates will be denoted by

$$\tau_{k_1, k_2, \ldots, k_i} = \tau_{k_1} + \tau_{k_2} + \ldots + \tau_{k_1} \qquad /2/$$

Note

A rectangular pulse shape was assumed for a simpler determination of propagation times as well as a more concise and clear description of the state of circuits considered in the paper. However it could be shown that all considerations are held, for instance for ramp pulses, as

well as for pulses of other shapes, in which the voltage changes /rising and falling parts/ occur in a monotonic way. In such cases the propagation times of the circuit gates should be appropriately defined.

4. Let the gate y, with propagation time τ_y, perform the function.

$$y = f(x_1, x_2, \ldots, x_i) \qquad /3/$$

Two states of gates will be distinguished

a. unstable state - from the time when the state of the gate inputs changed to the time τ_y after this change. At this time the zero-one input and output states may not satisfy the equation /3/,

b. stable state - after a time greater than τ_y since the last change of the gate input state. Zero-one input and output states satisfy the equation /3/.

The state of a circuit composed of many gates is called a stable one when all its gates are in a stable state. It is evident that if the state of any input of the circuit does not change, the output states of all gates will remain unchanged.

The time of the completion of the circuit operation may be defined as the time from the moment of the last change of the voltage levels on the circuit inputs to the moment of the stabilization of the state of all circuit gates. If the circuit does not comprise closed loops, the maximal time of the circuit completion may be estimated from its logical construction with a known τ_{max} time. The upper limit of this time is estimated as the product of a maximal number of circuit gates connected in series and of the time τ_{max}.

5. Assume, that the considered parallel binary adder satisfies following conditions:

a. the adder consists of n equal stages /n one-position adders/. One-positional adder, being the i-th stage of the parallel adder, has a_i, b_i, c_i inputs and s_i, c_{i+1} outputs. The stages are connected in such a way that point c_{i+1} is simultaneously the input of the $i+1$-st stage and the output of the i-th stage.

b. Every adder stage consists of gates performing simple logical functions /for instance, true or negated functions of the sum or the product of true and negated argument values - compare fig. 1/. Propagation times of every gate satisfy the condition /1/.

c. We assume the following operation of the considered adder:
On the adder inputs a_i, $b_i (i = 1, 2, \ldots, n)$ and c_1 the change of voltage levels, corresponding to bits of arguments of the operation, occurs at a certain moment.
At a certain time after the stabilization of voltage levels on the inputs a_i, $b_i (i = 1, 2, \ldots, n)$ and c_1, the voltage levels become stabilized on the adder outputs $s_i (i = 1, 2, \ldots, n)$. When the adder state is stabilized, voltage levels on the adder outputs $s_i (i = 1, 2, \ldots, n)$ correspond to the result bits $s_i (i = 1, 2, \ldots, n)$ of the adder operation.

d. There is no need to define either operations realized in the adder or functions performed by one-positional adders. It will be seen in examples, that the adder stages are adapted to add separate bits of two added numbers. It, however, is of no essential importance for the recognition methods presented in the paper.

In order to simplify considerations we shall divide the adder into three kinds of circuits

- Input circuits performing auxiliary functions being arguments of carry and result functions. For i-th stage performing the addition they may be, for instance, functions $a_i b_i$, $\bar{a}_i \bar{b}_i$, $\bar{a}_i b_i + a_i \bar{b}_i$.
- Carry circuit, consisting of gates connected in series and being a part of all adder stages. In this circuit carries c_{i+1} are functions of the carries c_i and of auxiliary functions performed in input circuits /see above/.
- Output circuits performing functions of the result s_i.

6. Other parallel adders will also be considered. They differ from those described in point 5, as their stages /one-positional adders/ may have pairs of inputs ^1c_i, ^0c_i and pairs of output s_i, $\bar{s}_i$ and $^1c_{i+1}$, $^0c_{i+1}$ instead of inputs c_i and outputs s_i, c_{i+1}.

This paper aims to define /the above assumptions being taken into account/ methods of recognition of parallel adder completion, after applying on its inputs a_i, b_i $(i = 1, 2, \ldots, n)$ the voltage levels, corresponding to the new combination of zeros and ones on which the operation is to be performed. In other words, the idea is to obtain the signalization of the correct operation result on outputs s_i $(i = 1, 2, \ldots, n)$ as early as possible.

The recognition of the adder completion should consist in the examination of the adder s_i $(i = 1, 2, \ldots, n)$ outputs completion. However, since the carry completion time dominates the addition time of the adder, and since the delay times of the input and output functions are practically constant, the addition time may be determined from the carry completion time.

The solution of the recognition circuit of the adder completion, adjoined to the adder, may be based on the following:

a. Some adequately chosen points of the adder may accept determined zero-one states only as a result of operation completion of the proper adder parts.

b. The completion of certain adder parts may be concluded, if voltage changes on the outputs of appropriate gates do not appear during the determined time.

Both these features require a more detailed discussion which will be presented in chapter 4 together with the discussion about proper recognition methods.

Now, we shall only draw attention to a certain fact connected with point a.

Assume, that the state of the output pair s_i, $\bar{s}_i$ /or a pair of points $^1c_{i+1}$, $^0c_{i+1}$/ of the i-th adder stage is 0, 0 before the completion of the state, and 0, 1 or 1, 0 after its

completion. Such states /0, 1 or 1, 0/ may be used to investigate the stage completion if they do not appear temporarily before its final completion. In the author's opinion this may be obtained if the solution of the adder ensures at the utmost a onefold voltage change on the output of each gate during the completion of the adder. This condition not being satisfied results in erroneous solutions of completion recognition in papers [4], [2] and [3] - as shown in chapter 3.

3. EXAMPLES OF ERRONEOUS OPERATION OF RECOGNITION CIRCUITS

Gate propagation times in a determined digital technique may largely fluctuate within the limits of condition /1/, and may differ many times even for the same gate type. We shall accept that the recognition circuit of the adder completion is solved erroneously if, with assumptions accepted in chapter 2, the propagation times for proper adder gates can be chosen so as to provide the signalization of the adder completion before its real completion. The voltage states on adequate gates of the considered adders will be shown by means of timetables.

Example 1

In I. Flores's paper [4], page 113, a scheme of one adder stage is presented. The recognition of the adder completion is based on the investigation of the carry circuit completion. One stage of the adder /ref. [4] /, together with the appropriate part of the recognition circuit, is shown in fig. 2a. The initial zero-state of the adder inputs is assumed.

The addition begins after a simultaneous applying of voltage levels, corresponding to the bits a_i, b_i $(i = 1, 2, \ldots, n)$ on all adder inputs. The recognition of the adder completion is based on the investigation of states of the pairs ${}^1c_{i+1}$, ${}^0c_{i+1}$ $(i = 1, 2, \ldots, n)$ of the carry circuit. The circuit signalizes the adder completion when none of the pairs ${}^1c_{i+1}$, ${}^0c_{i+1}$ takes the values 0, 0.

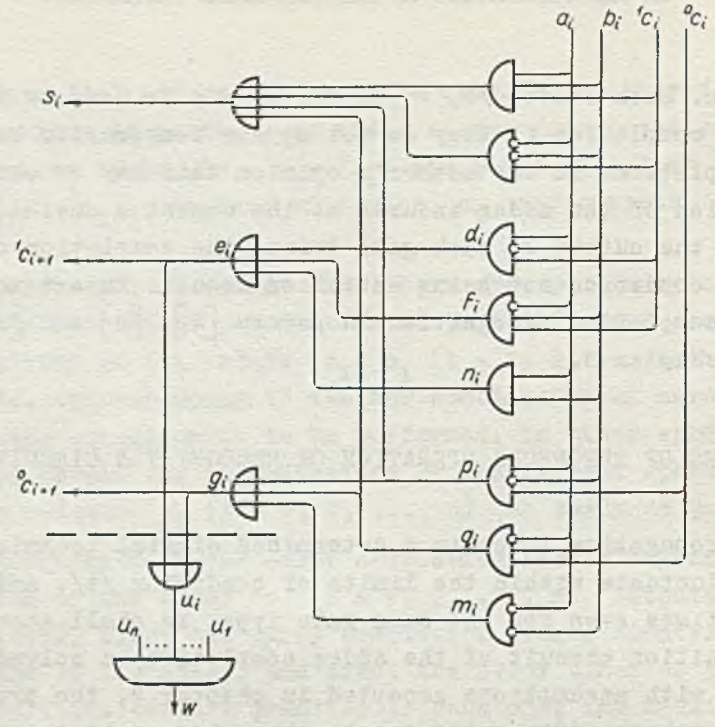


Fig. 2a. One adder stage and recognition circuit stage for the adder from paper [4].

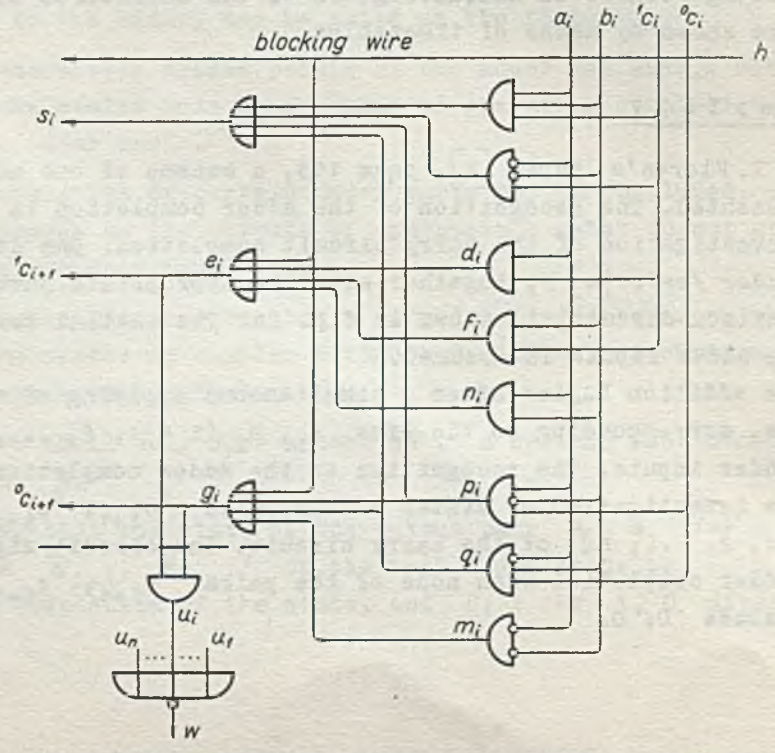


Fig. 2b. Modified version of the circuit presented in fig. 2a.

Let us consider a four-positional adder in which the propagation time of each gate is t $(t < \tau_{max})$. For adding four bit numbers, in which

$$a_1 = 1 \quad a_2 = 1 \quad a_3 = 1 \quad a_4 = 1$$
$$b_1 = 1 \quad b_2 = 0 \quad b_3 = 0 \quad b_4 = 0 \qquad \left({}^1c_1 = 0,\ {}^0c_1 = 1\right)$$

the timetable of some output states of the gates is shown in fig. 3a. It follows from the timetable that the state of each pair ${}^1c_{i+1}$, ${}^0c_{i+1}$ $(i = 1, 2, \ldots, n)$ is every moment 0, 1 or 1, 0 during the whole period of the process of carry completion. Thus, the operation of the recognition circuit is erroneous.

Example 2

In J.Sklansky's paper [2] the IDA /the independent-dependent carry adder/ is described. The recognition of the adder completion is based on the examination of the completion of carry propagation in the carry circuit, one stage of which, together with a proper part of the recognition circuit, is shown in fig. 4a. The initial zero-state of the adder inputs is assumed.

Addition starts after the values a_i, b_i $(i = 1, 2, \ldots, n)$ have been simultaneously fed to all adder inputs. The recognition is based on the investigation of the states of pairs ${}^1c_{i+1}$, ${}^0c_{i+1}$ $(i = 1, 2, \ldots, n)$ of the carry circuit. The circuit signalizes the adder completion when none of the pairs ${}^1c_{i+1}$, ${}^0c_{i+1}$ takes the values 0, 0.

An erroneous signalization of the addition completion may occur in the IDA, for instance, if for several subsequent stages /fig.4a/ the gate propagation times satisfy the dependence

$$\tau^i_{q,r,f} \leq \tau^i_m \quad \text{or} \quad \tau^i_{p,r,f} \leq \tau^i_m \qquad /4/$$

Let us consider a four-positional adder with gate propagation times

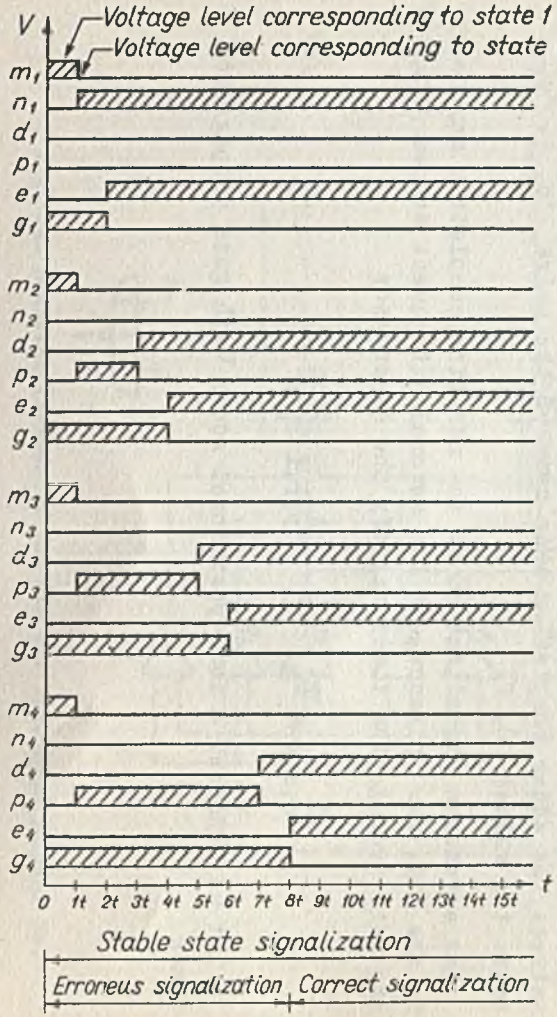


Fig. 3a. Timetable for example 1

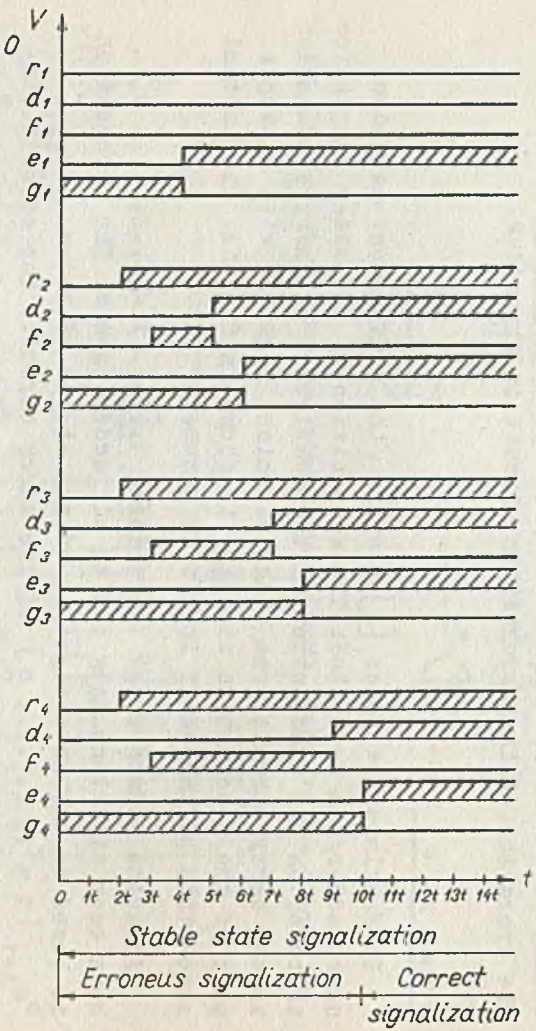


Fig. 3b. Timetable for example 2

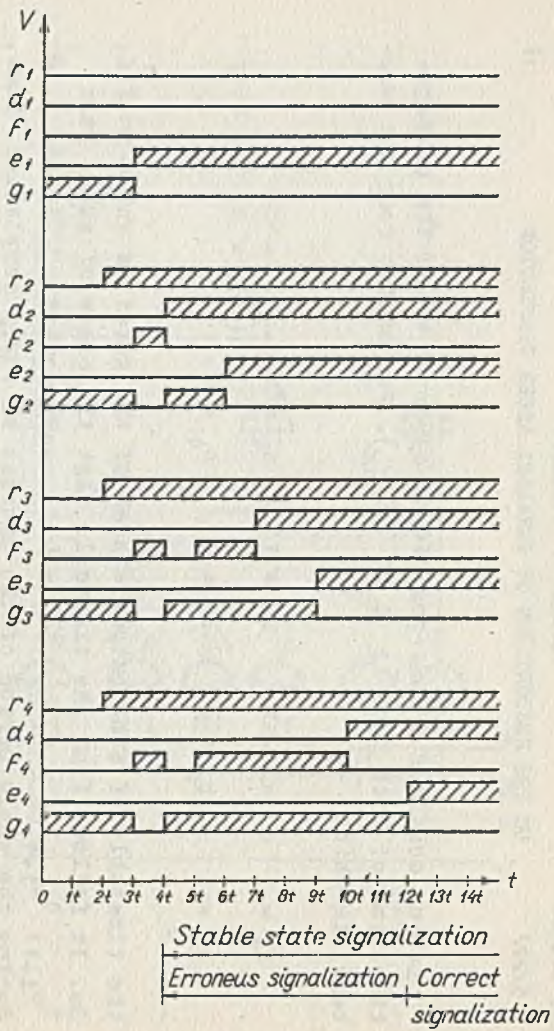


Fig. 3c. Timetable for example 3

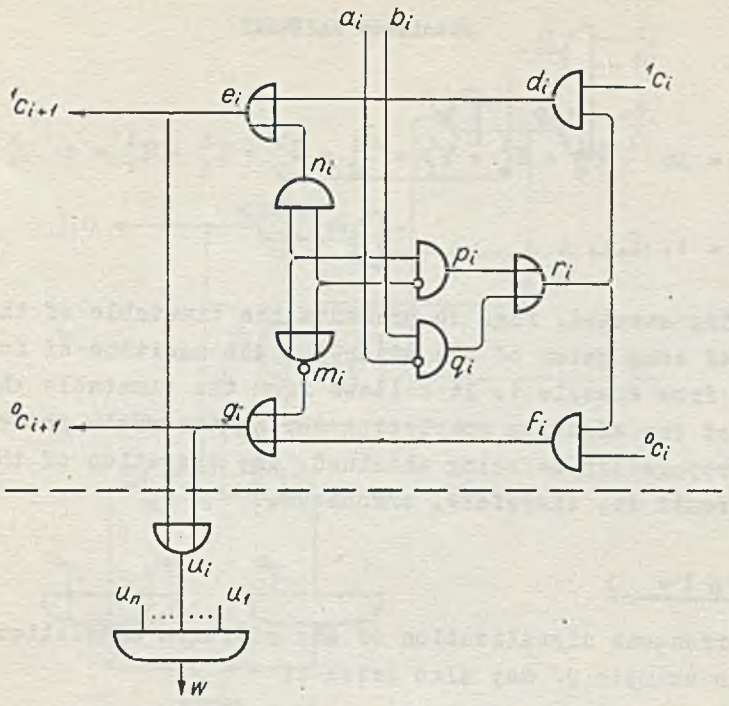


Fig. 4a. One carry circuit stage and recognition circuit stage for the adder IDA paper [2].

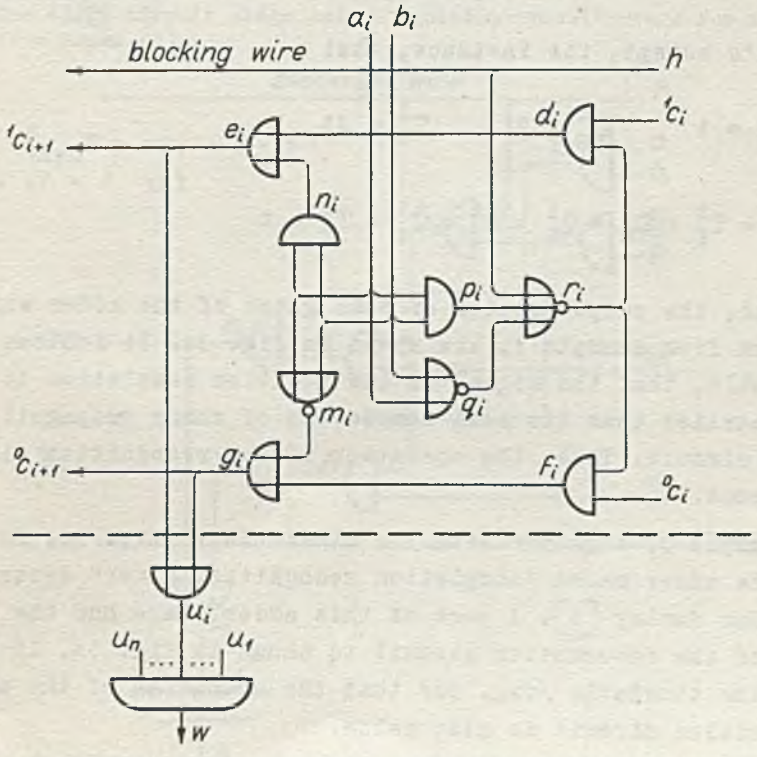


Fig. 4b. Modified version of the circuit presented in fig. 4a.

$$\tau_n^i = \tau_m^i = 3t \qquad \tau_d^i = \tau_e^i = \tau_f^i = \tau_g^i = \tau_p^i = \tau_q^i = \tau_r^i = t \qquad (3t < \tau_{max})$$

for $i = 1, \ldots, 4$

This being assumed, fig. 3b presents the timetable of the output states of some gates of the adder for the addition of four-bit numbers from example 1. It follows from the timetable that the signal of the addition completion during the whole process of the carry propagation is being obtained. The operation of the recognition circuit is, therefore, erroneous.

Example 3

An erroneous signalization of the addition completion in the IDA /ref. to example 2/ may also arise if

$$\tau_{+g} < \tau_{-g} \qquad /5/$$

Let's accept, for instance, that

$$\tau_{+g}^i = t \qquad \tau_{-g}^i = 2t \qquad \tau_e^i = 2t \qquad (2t < \tau_{max})$$

$$\tau_d^i = \tau_f^i = \tau_m^i = \tau_n^i = \tau_p^i = \tau_q^i = \tau_r^i = t \qquad \text{for } i = 1, \ldots, 4$$

Then, the output states of some gates of the adder while adding numbers from example 1, are shown in fig. 3c. It follows from the timetable, that the signal of the addition completion is obtained much earlier than the real completion of carry propagation in the carry circuit. Thus, the operation of the recognition circuit is erroneous.

Example 3, together with the timetable in fig. 3c, fully holds for the adder named "completion recognition adder" described by O.L. Mac Sorley [3]. A part of this adder stage and the proper part of the recognition circuit is shown in fig. 5a. It follows from the timetable /fig. 3c/ that the operation of the adder state recognition circuit is also false.

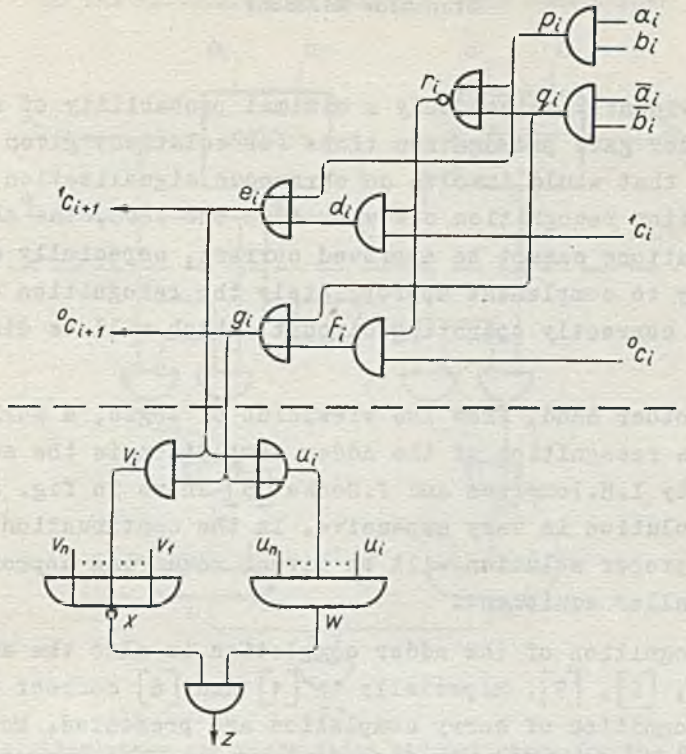


Fig. 5a. One carry circuit stage and recognition circuit stage for the adder from paper [3].

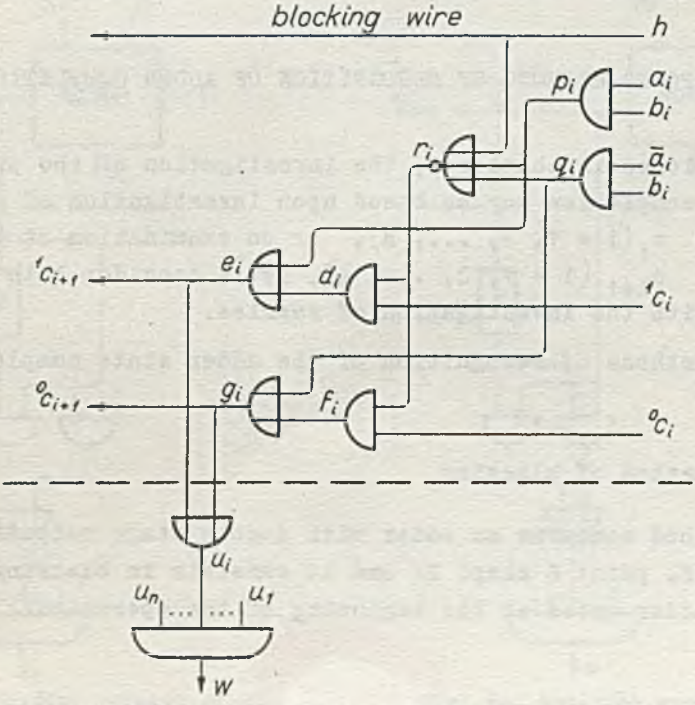


Fig. 5b. Modified version of the circuit presented in fig. 5a.

There evidently exists only a minimal probability of such selection of adder gate propagation times for solutions given in fig.2a, 4a and 5a, that would involve an erroneous signalization of the adder completion recognition circuit. None the less, the above-mentioned solutions cannot be approved correct, especially as it is rather easy to complement appropriately the recognition circuit and gain a correctly operating circuit, which will be discussed further.

On the other hand, from the viewpoint of logic, a correct solution of the recognition of the adder completion is the solution presented by I.H.Pomerene and J.Cocke [5] shown in fig. 6a. But this solution is very expensive. In the continuation of this paper the proper solution will be given, requiring approximately a twice smaller equipment.

The recognition of the adder completion is also the subject of papers [1], [6], [7]. Especially in [1] and [6] correct methods of the recognition of carry completion are presented. Moreover, in [6] and [7] the methods of evaluation of mean values of carry propagation time are discussed.

4. THE PROPOSED METHODS OF RECOGNITION OF ADDER COMPLETION

As mentioned in chapter 2, the investigation of the process of the adder completion may be based upon investigation of adder output states $s_i (i = 1, 2, \ldots, n)$, or on examination of the states of carries $c_{i+1} (i = 1, 2, \ldots, n)$. Let's consider both versions starting with the investigation of carries.

Three methods of recognition of the adder state completion are presented.

4.1. The method of blocking

The method concerns an adder with double stage outputs ${}^1c_{i+1}$, ${}^0c_{i+1}$ /ref. point 6 chap. 2/ and it consists in blocking properly selected adder gates at the beginning of the operation.

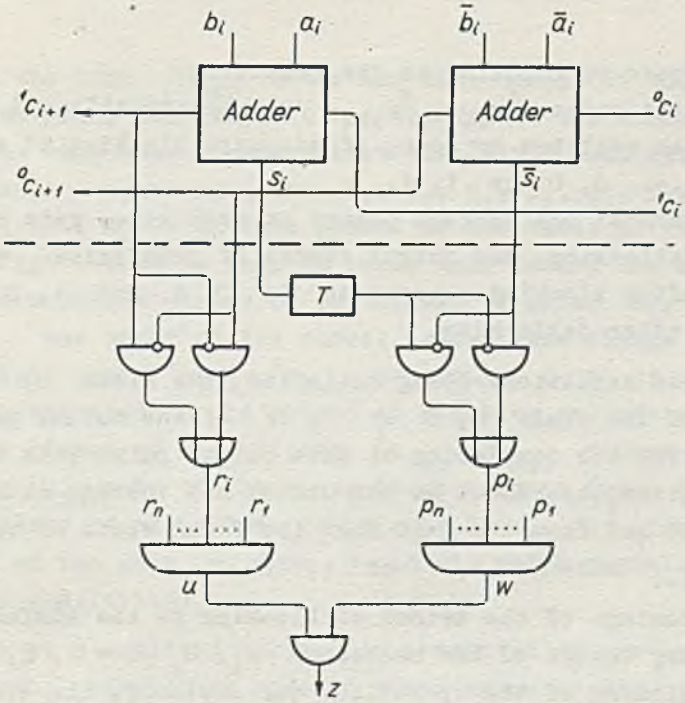


Fig. 6a. One adder stage and recognition circuit stage for the adder from paper [5].

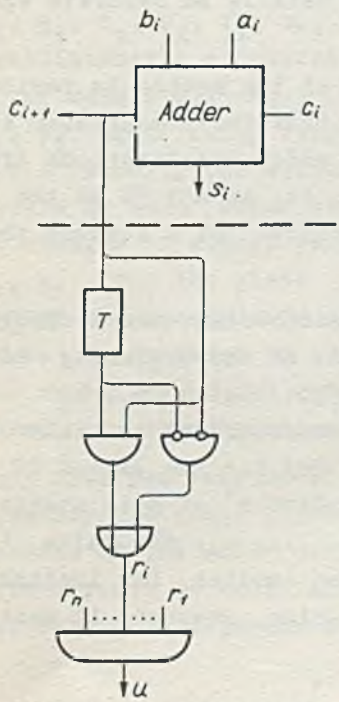


Fig. 6b. Modified version of the circuit presented in fig. 6a.

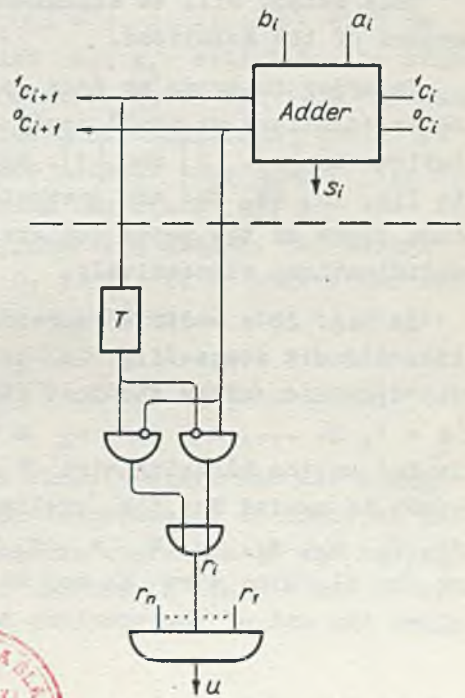


Fig. 6c. Modified version of the circuit from fig. 6a for another type of the adder.

The purpose of blocking is the following:

1. The output pairs $^{1}c_{i+1}$, $^{0}c_{i+1}$ /not necessarily all of them/ should be switched by means of adequate blocking to an equal state i.e. 0, 0 or 1, 1.
2. At the utmost one voltage change on each adder gate may occur after deblocking. The output states of gate pairs $^{1}c_{i+1}$, $^{0}c_{i+1}$ which after blocking correspond to 0, 1 and 1, 0 cannot change after deblocking.

The above conditions being satisfied, the state 0, 1 or 1, 0 /instead of the state 0, 0 or 1, 1/ of the output pair $^{1}c_{i+1}$, $^{0}c_{i+1}$ proves the completion of this output pair. This follows from the assumption about at the utmost one voltage change on each gate output and from the fact that the final state of the pair $^{1}c_{i+1}$, $^{0}c_{i+1}$ must be 0, 1 or 1, 0.

The advantage of the method of blocking is the admissibility of an arbitrary change of the states of a_i, b_i $(i = 1, 2, \ldots, n)$ at the beginning of the operation, for instance, the zeroing of adder inputs is not necessary.

This method will be explained more in details on concrete examples of the solutions.

In order to prove an easy application of the method to various adder solutions we shall apply it to the proviously mentioned solutions in [4], [2] and [3]. Appropriate adder modifications /ref. to fig. 2a, 4a, 5a/ are presented in fig. 2b, 4b and 5b on the same pages of the paper for easier comparison. Let's discuss these modifications successively.

In fig. 2b a modified version of one adder stage and a recognition circuit stage /fig. 2a/ is presented. At the beginning of the operation after the last change of input states a_i, b_i $(i = 1, 2, \ldots, n)$ and c_1 a voltage corresponding to state 1 is fed on the blocking wire h /see fig. 2b/ for the period $2\tau_{max}$, which is needed for the 'preliminary completion' of gate states d_i, f_i, n_i, p_i, q_i, m_i, e_i, g_i $(i = 1, 2, \ldots, n)$. The value 1 on the blocking wire h may be also given earlier, for instance, after the end of the previous adder operation. However, it must

last till the time $2\tau_{max}$ after the last change of the adder input states. Next, the state 0 is applied to the blocking wire h. This is the very moment after which the 'final completion' of the carry circuit comprising gates d_i, f_i, n_i, p_i, q_i, m_i, e_i, g_i $(i = 1, 2, \ldots, n)$ will take place. On the basis of the scheme shown in fig. 2b, it is easy to check that during the carry circuit completion a single change of the states of gates d_i, f_i, e_i or p_i, q_i, g_i may occur at the utmost. After this change the state of the output pair $^1c_{i+1}$, $^0c_{i+1}$ is always 0, 1 or 1, 0. The conditions required in the method of blocking are satisfied. The zero-state of one of the outputs $^1c_{i+1}$, $^0c_{i+1}$ causes the switching of the u_i gate of the recognition circuit from 1 to 0. The zero-state of all gates u_i $(i = 1, 2, \ldots, n)$ causes the switching of the gate w from 0 to 1 which signalizes the carry circuit completion.

In fig. 4b a modified version is presented of one carry circuit stage and the recognition circuit stage shown in fig. 4a. After the change of the input states a_i, b_i $(i = 1, 2, \ldots, n)$ and c_1, $h = 1$ is kept for the period $3\tau_{max}$. Then the state of the gates p_i, q_i, r_i, d_i, f_i, m_i, n_i, e_i, g_i $(i = 1, 2, \ldots, n)$ will be 'preliminarily completed'. The pairs e_i, g_i will take the states 0, 0 relatively 0, 1 or 1, 0; states 0, 1 or 1, 0 of gates e_i, g_i are finally completed. After deblocking from $h = 1$ to $h = 0$ exactly one switching of gate outputs d_i, e_i or f_i, g_i occurs in such adder stages in which the state e_i, g_i was 0, 0. No changes of states occur in the remaining stages. The change e_i, g_i from the state 0, 0 to 0, 1 or 1, 0 causes the switching of the recognition circuit gate u_i from 0 to 1 state. State 1 achieved on all gates u_i $(i = 1, 2, \ldots, n)$ effects the switching of the gate w from 0 to 1 which signalizes the carry circuit completion.

A modified version of one carry circuit stage and the recognition circuit stage given in fig. 5a is presented in fig. 5b. The process of the adder completion and the operation of the recognition circuit is fully analogous to the one in fig. 4b and it does not require a separate description.

The completion of the adder carry circuit in all above-mentioned solutions may occur earlier than the completion of the output states s_i $(i = 1, 2, \ldots, n)$. The time of preceding may, for instance, be evaluated by the time τ_{max} or the time $2\tau_{max}$ depending on the realization of circuit of the funotion s_i. This should be taken into account in the adder control if the content of the adder outputs is transferred to other computer circuits immediately after the end of the adder operation.

More economical recognition circuits may be obtained by reducing the number of checked pairs of the adder outputs $^1c_{i+1}$, $^0c_{i+1}$ and testing only every N-th output pair. Such a reduction of the checked pairs is convenient, for instance, in the case of a necessary limitation of the gate input number /ref. gate w in fig. 2b, 4b and 5b/. In this case the signal of completion is generally obtained earlier than the real end of carry propagation. The time of the preceding does not exceed the time of the completion of N-1 carry circuit stages and, for instance, for the solutions in fig. 2b, 4b, 5b it may be $2(N-1)\tau_{max}$. One should add to this time the one needed for the completion of the output states s_i $(i = 1, 2, \ldots, n)$, which is dependent on the adder solution and usually not exceeding $2\tau_{max}$.

In certain cases the signalization preceding the operation end may be advantageous as it provides some additional time reserve for the control of the next operation. In solutions where we want to obtain the signal after the real operation end, an adequate delay should be added on the recognition circuit output.

The number of the blocked adder gates may also be reduced and, for example, only every M-th stage may be blocked. The period of blocking should then be prolonged approximately for a maximal time of operation of M-positional adder. For adders fig. 2b, 4b and 5b, this time is respectively $2M\tau_{max}$, $(2M+1)\tau_{max}$ and $(2M+1)\tau_{max}$.

The recognition of the adder state may also be based, as mentioned at the beginning of the chapter, on the examination of the completion of adder outputs s_i, $\bar{s}_i$ $(i = 1, 2, \ldots, n)$.

Assume, that functions s_i, $\bar{s}_i$ are performed in one positional adders on the basis of formulas

$$s_i = \bar{r}_i \, {}^1c_i + r_i \, {}^0c_1 \qquad /6/$$

$$\bar{s}_i = r_i \, {}^1c_i + \bar{r}_i \, {}^0c_i \qquad /7/$$

where

$$r_i = \bar{a}_i \, b_i + a_i \, \bar{b}_i \qquad /8/$$

Then, the state 0, 0 or 1, 1 of the pair of outputs ${}^1c_i$, ${}^0c_i$ consequently causes the state 0, 0 or 1, 1 on outputs s_i, $\bar{s}_i$. It is easy to check in formulas /6/ and /7/ that a single change of the state of outputs ${}^1c_i$, ${}^0c_i$ causes a single change of the state of outputs s_i, $\bar{s}_i$. Therefore, if blocking is applied as described for solutions in fig. 2b, 4b and 5b, the states of the adder outputs s_i, $\bar{s}_i$ $(i = 1, 2, \ldots, n)$ satisfy all conditions required in the method of blocking for the recognition of the adder oompletion. The recognition circuit, being identical to those in examples fig. 2b, 4b and 5b, may thus be adjoined to the adder outputs s_i, $\bar{s}_i$ $(i = 1,2, \ldots, n)$. Separate performance of the function $\bar{s}_i$ on the basis of formula /7/, independently of the function s_i requires, however, a larger equipment than, for instance, the performance of the function $\bar{s}_i$ as the negation s_i. This is the solution disadvantage. The second disadvantage is an additional charge of outputs s_i, $\bar{s}_i$ $(i = 1, 2, \ldots, n)$ by the recognition circuit, as these outputs are usually charged with many other circuits. On the other hand, the obtaining of the signalization of the completion recognition after a real adder completion may be its advantage.

In this case more economical recognition circuits may also be applied by means of investigating the states of the outputs s_i, $\bar{s}_i$ of every N-th stage. The signalization of the adder completion may then precede the real operation end. The blocking of the adder gates may also be reduced to every M-th stage. Then, of course the time of blocking is required to be prolonged.

4.2. The method of delay lines

Assume that in the adder described in point 5 chapter 2, the maximal number of gates connected in series in one stage is k. Then, the time

$$T = k\tau_{max} \qquad /9/$$

is the maximal time of one stage completion.

The method of delay lines is based upon the following:

If during a certain period T, after the last change of the state of inputs a_i, b_i /not necessarily directly after this change/, the state of input c_i does not change, then after this period the i-th adder stage is completed. If during a certain period T after the last change of the state of the inputs a_i, b_i $(i = 1, 2, \ldots, n)$ /not necessarily directly after this change/ the state of none of the input c_i $(i = 1, 2, \ldots, n)$ changes, then the whole adder is completed.

If in the course of the adder completion in each of the points c_{i+1} $(i = 1, 2, \ldots, n)$ at the utmost a single voltage change occurs, then the adder completion may be recognized by means of the recognition circuit shown in the scheme in fig. 6b. This, for instance, may occur if a single change of the adder input states from zero-states to the values a_i, b_i $(i = 1, 2, \ldots, n)$ and c_i appears and functions c_{i+1} $(i = 1, 2, \ldots, n)$ are realized according to

$$c_{i+1} = a_i b_i + a_i c_i + b_i c_i \qquad /10/$$

At most a single change of c_{i+1} $(i = 1, 2, \ldots, n)$ output states is then obtained. In other words, if arbitrary arguments a_i, b_i, c_i of the function c_{i+1} /see /10// change from zero-states in an arbitrary succession at the utmost once, this causes at the utmost one change of the function c_{i+1}.

It follows from fig. 6b that a single change of the c_{i+1} output state causes the appearance of zero on the output of gate r_i during the period T. The end of the adder completion is signalized by the state of the output of the gate u, being the result of state 1 of all gate outputs r_i $(i = 1, 2, \ldots, n)$. A correct signalization of the operation end is obtained at the latest after the time $T + 3\tau_{max}$ since the last change of outputs c_{i+1} $(i = 1, 2, \ldots, n)$ /the time $3\tau_{max}$ is the maximum propagation time of three gates connected in series in the recognition circuit/.

The circuit presented in fig. 6b is approximately twice as economical as the circuit in [5] shown in fig. 6a, which results from schemes 6a and 6b.

If the adder stages have, besides outputs $^1c_{i+1}$, also outputs $^0c_{i+1}$ the recognition circuit presented in fig. 6c may be used instead of that in fig. 6b. This circuit has an additional advantage, namely it lacks the signal of the operation end if the states of the adder stage outputs $^1c_{i+1}$, $^0c_{i+1}$ are equal, which may result from the adder damage.

More economical recognition circuits may be obtained by reducing the number of checked adder stages. For instance, one may check every N-th stage by exchanging the T delay lines into NT delay lines. Maximal delay of the signal of the operation end in an adder may then be $NT + 3\tau_{max}$.

For the recognition of the adder completion the outputs s_i, or the outputs s_i and $\bar{s}_i$ may also be used instead of outputs c_{i+1}, or $^1c_{i+1}$ and $^0c_{i+1}$. But the recognition circuit operates correctly for single voltage steps, and the state of outputs s_i and $\bar{s}_i$ may change several times. This fact may, however, be easily taken into account. The majority of the adders are solved so that after the time T the state of adder stage is 'preliminarily completed', and it may later be changed only once, as a result of a single change of the c_i input state. In this case the recognition circuit gives a correct signal after the time $2T + 3\tau_{max}$ from the beginning of the operation.

The former notes on more economical recognition circuits, checking only every N-th stage of the adder, are fully held in the last case of investigation of outputs s_i, or s_i and $\bar{s}_i$ instead of outputs c_{i+1}, or $^1c_{i+1}$ and $^0c_{i+1}$.

4.3. The method of differentiators

This method being a modification of the method of delay lines, is based on the assumptions on step changes of outputs c_{i+1} $(i = 1, 2, \ldots, n)$ and the maximal time T of adder stage completion. The method does not require either the initial zero-state of inputs a_i, b_i $(i = 1, 2, \ldots, n)$ or the assumption of single voltage changes.

The recognition circuit of the adder completion consists of:

a/ n differentiators that change the voltage steps into narrow pulses
b/ circuits that widen the pulses to the width T.
c/ n - arguments or-gate

The operation of the recognition circuit connected with the adder outputs c_{i+1} $(i = 1, 2, \ldots, n)$ is based upon the fact that the changes of the states c_{i+1} $(i = 1, 2, \ldots, n)$ during the adder operation do not appear more seldom than every period T. If these changes cause the arising of pulses on the outputs of differentiators which are later widened to the width T, then their logic sum /inclusive or/ will equal 1 during the whole adder operation. To say it more exactly, the signalization may be somewhat delayed /at the maximum by the time T increased by the time of signal propagation of the recognition circuit/. The timetable of the recognition circuit operation is shown in fig. 7.

The performance of the recognition circuit is very simple in many techniques, as the widened pulses may often be reached in one circuit after summing up the narrow pulses gained from differentiator outputs.

The recognition circuit discussed may also be adjoined to the adder outputs s_i, instead of outputs c_{i+1}.

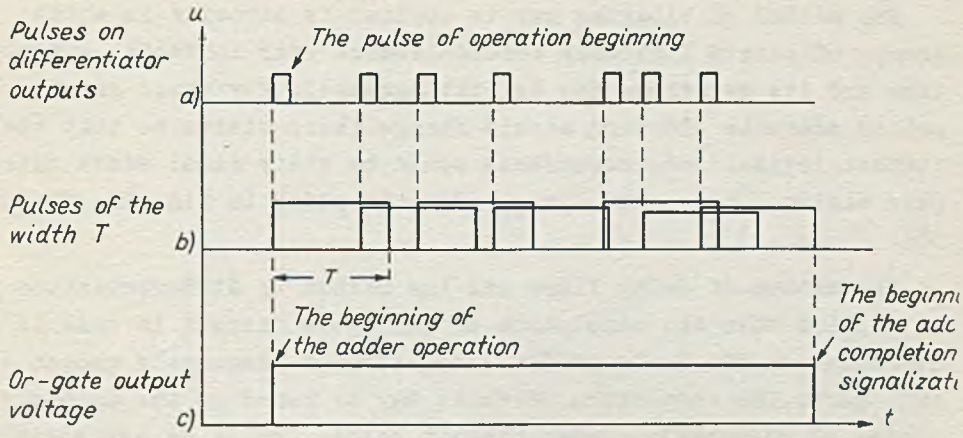


Fig. 7. Timetable of the recognition circuit operation.

In this method, like in the former, more economical recognition circuits may be applied. Only every N-th stage may be checked by means of pulses of the width NT instead of those of the width T. The adder operation end is then signalized by the recognition circuit with a maximal delay NT plus the time of signal propagation of the recognition circuit.

5. CONCLUSIONS

The principles of the adder completion recognition, formulated in the present paper, may be applied to various adder solutions. Examples were presented only for comparison with solutions in papers [4], [2], [3], [5].

Only adders consisting of equal stages /equal one-positional adders/ were considered. None the less, the presented methods are suited for the recognition of the completion of a larger class of adders.

It seems that the described recognition methods of the adder completion may also be transferred to certain other asynchronous digital circuits, not containing closed loops.

The method of blocking may be applied to circuits in which groups of points logically interdependent /for instance, a function and its negation/ may be distinguished. For these groups of points adequate blocking should change their states so that their correct logical interdependence would be their final state /compare states $^{1}c_{i+1}$ and $^{0}c_{i+1}$ for the adder in fig. 2b, 4b and 5b/.

The method of delay lines and the method of differentiators may be applied when the completion of the whole circuit is easy to be concluded on the basis of the completion of adequately chosen circuit parts, the completion of which may be based on the unchanged states of adequately chosen circuit points during an appropriate time period.

Acknowledgement

The author wishes to express his thankfulness to Prof. Dr. L. Łukaszewicz, Docent Dr Z. Pawlak and Mr. J. Fiett for their valuable remarks and suggestions as well as for fruitful discussions on many problems considered in the paper.

References

1. GILCHRIST B., POMERENE J.H., WONG S.Y.: Fast Carry Logic for Digital Computers, IRE Trans. on Electronic Computers, December 1955:EC-4, 133-136.

2. SKLANSKY J.: An Evaluation of Several Two-Summand Binary Adders, IRE Trans. on Electronic Computers, June 1960:EC-9, 2, 213.

3. MAC SORLEY O.L.: High-Speed Arithmetic in Binary Computers, Proceedings of the IRE, January 1961:49, 1, 67.

4. FLORES I.: The Logic of Computer Arithmetic, Prentice-Hall, INC., 1963:70-82, 113-114.

5. POMERENE J.H., COCKE J.: Asynchronous Adder-Subtractor System, United States Patent Office 3051387, Patented August 1962.

6. HENDRICKSON H.C.: Fast High-Accuracy Binary Parallel Addition, IRE Trans. on Electronic Computers, December 1960:EC-9, 4, 465-468.

7. REITWIESNER G.W.: The Determination of Carry Propagation Length for Binary Addition, IRE Trans. on Electronic Computers, March 1960:EC-9, 1, 35-38.