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ON CHECKING ONE-PULSE NETWORKS

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It is characteristic of many control networks in digital computers that exactly one element of the network is active at any moment during their operation. Several methods of checking such a one-pulse network operation are described in the present paper. The principle of recognition of the sum of pulses, in a determined moment in N points of the network, being exactly 1, is evidently simple. However, the effectiveness of the checking circuit operation, as well as economical limitations, permit to apply exclusively small circuits with a very simple logic as compared with the checked network. This is of special importance in the case of larger networks. The methods presented in the paper permit to realize relatively small and, in the author's opinion, effective checking circuits.

1. DEFINITIONS AND DENOTATIONS

The described electronic digital circuits will be considered entirely in discrete, consecutively numbered time periods T.

The e l e m e n t a r y c i r c u i t will be called such an electronic circuit which delays by the period T, on the output of which a determined zero-one function of arguments given on its inputs is realized. The zero-one output state of the elementary circuit i at the moment t /i.e. at the t-th period T/ will be denoted by a_i^t.

The connection of the output of the elementary circuit i with the input of the elementary circuit j will be denoted by $c_{ij} = 1$; the lack of such a connection - by $c_{ij} = 0$.

The n e t w o r k will be the term of the set of connected N elementary circuits.

We shall confine ourselves to disouss the circuit checking for a network, composed of N elementary circuits, with the following properties:

a/ elementary circuits of the network realize zero-one functions

$$a_j^{t+1} = \sum_{i=1}^{N} {}^{\vee} c_{ij}\, b_{ij}^t\, a_i^t \qquad \text{for } i = 1, 2, \ldots, N \text{ and for every } t \qquad /1/$$

where

- symbol $\sum^{\vee}$ denotes the inclusive or function
- b_{ij}^t denotes zero-one state of input of the elementary circuit j connected with the outputs of circuits being beyond the investigated network. This b_{ij}^t factor determines the influence of the circuits from outside of the examined network at the moment i upon its operation.

b/ zero-one states b_{ij}^t satisfy the condition

$$\sum_{j=1}^{N} c_{ij}\, b_{ij}^t = 1 \qquad \text{for } i = 1, 2, \ldots, N \text{ and for every } t \qquad /2/$$

where symbol $\sum$ denotes the arithmetic sum.

A network with such properties will be called o n e - p u l s e n e t w o r k for it follows from /1/ and /2/ that if at the moment τ

$$\sum_{i=1}^{N} a_i^{\tau} = 1 \qquad /3/$$

then for every moment $t > \tau$ also

$$\sum_{i=1}^{N} a_i^t = 1 \qquad /4/$$

We shall assume that in every correctly operating one-pulse network the condition /4/ is always satisfied.

The appearing of an e r r o r in one-pulse network at the moment $\tau + 1$ takes place if there exists such integer $j(1 \leq j \leq N)$ for which the equation /1/ for $t = \tau$ is not satisfied.

The appearing of a · s i n g l e e r r o r at the moment $\tau + 1$ takes place if there exists striotly one integer $j(1 \leq j \leq N)$ for which the equation /1/ for $t = \tau$ is not satisfied.

Note.

It follows from /2/ that the output of every elementary circuit of a one-pulse network is connected with an input of at least one elementary circuit of the network. Especially, if the output of the elementary circuit i is connected with its input, i.e. $c_{ii} = 1$ then the circuit is a storing one.

2. METHODS OF FAST ERROR DETECTION

The ohecking of the network operation will be based on the investigation of the condition /4/. From a practical viewpoint these methods of error deteotion are interesting for whioh the checking circuits are

a/ relatively small and simple as compared with the checked network,

b/ relatively effective, i.e. they detect a relatively large number of cases of an erroneous network operation.

Moreover, the signalization should follow appropriately fast after the appearance of the error, although it is often less important than the effectiveness of an operation of the checking circuits.

Several checking methods are presented below including for comparison those which do not satisfy the above conditions.

1. A checking method based on examination whether "ones" do not appear simultaneously on outputs of an even number of elementary circuits. The checking circuit for an N element network consists of $N - 1$ exclusive or gates. The error is signalized if any odd number of single errors appears in the checked network.

2. A checking method based on examination whether any "one" exists on outputs of network elementary circuits or whether "ones" do not exist on more than one elementary circuit output.

   The checking circuit consists of

   a/ or-gate and its negation of outputs of all elementary circuits for detecting the zero-state /lack of "ones"/ of the network.

   b/ N circuits, consisting of an and-gate of one elementary circuit output and of an or-gate of the outputs of the remaining elementary circuits in all possible combinations. Every and-gate detects the presence of a "one" in a selected elementary circuit and simultaneously in an arbitrary one, among the remaining circuits. These circuits may be appropriately simplified depending on the applied technique.

   c/ the $N + 1$ argument or-gate of the outputs of circuits mentioned in points a/ and b/.

   The size of such checking circuit is approximately proportional to the square of the number of elementary circuits of the checked network. Such checking circuit is rather complex, particularly for a network with a big number of elementary circuits.

3. The checking method based on examination whether "ones" do not simultaneously appear on outputs of directly connected elementary circuits.

   The detection circuit consists of

   a/ or-gate and its negation for detecting the absence of "ones" in the network as in method 2,

   b/ two-argument and-gates for all pairs of elementary circuits i, j for which $c_{ij} = 1$,

c/ the or-gate of outputs of all gates given in points a/ and b/.

It follows from the one-pulse network definition that every change of the network state is the change of states of two elementary circuits being directly connected. When assuming that an erroneous operation of elementary circuits most frequently occurs during the change of their states, it is sufficient to check whether "ones" are not simultaneously present in directly connected elementary circuits. Such a checking is made by two-argument and-gates /point b//.

4. The method, as in point 3, with simplified checking circuits.

The checking circuits may be often considerably simplified depending on the structure of the network and the technique used.

Assume, for instance, a construction of a one-pulse network permitting to number its elementary circuits in such a way that, besides the storing connections of separate elementary circuits, every connection joins the even elementary circuit with the odd one. For such a network all and-gates of the point b/ of method 3 and their or-gate may be replaced by the or-gate of outputs of even elementary circuits, the or-gate of outputs of odd elementary circuits and their two argument and-gate. An admission of a small number of connections between even or between odd elements of the network causes only the addition of the same number of two-argument and-gates to the checking circuit.

The elementary circuit that stores the signal of error detection has not been taken into account in the above discussed methods. This note concerns the method presented in the next chapter as well.

3. THE METHOD OF A DELAYED DETECTION OF ERROR.

The following assumptions will be accepted, not being essential for the above described methods

a/ we shall consider only the detection of random errors. /The detection of permanent errors is usually easier/,

b/ we shall assume great reliability of the network operation. Therefore errors occur seldom, and the frequency of their appearance exceeding one error during the period needed for error detection may be neglected. For the method given below and for the cyclic network operation, this assumption is equivalent to the fact that the cycle of the network operation is many times shorter than the rate of error occurring in the network.

The method of a delayed error detection is a modification of method 2 from the previous chapter.

Let's consider one of the and-gates of the point b/, method 2 from chapter 2, namely the and-gate of the output of the elementary circuit i and the output of or-gate of the remaining elementary circuit outputs.

This and-gate signalizes the error if at the moment τ

$$a_i^{\tau}\left(\sum_{j=1}^{i-1}{}^{\vee} a_j^{\tau} \vee \sum_{j=i+1}^{N}{}^{\vee} a_j^{\tau}\right) = 1 \qquad /5/$$

where the symbol $\vee$ denotes an inclusive-or function i.e. when there simultaneously is a "one" on the output of the elementary circuit i and a "one" on the output of another arbitrary elementary circuit of the network. One such an and-gate is already an efficient circuit, detecting the state

$$\sum_{j=1}^{N} a_j^{t} > 1$$

if:

a/ there exists in the network an elementary circuit i, on the output of which "one" appears sufficiently often,

b/ the state

$$\sum_{j=1}^{N} a_j^t > 1$$

holds for the network for the period of time, in which a "one" appears at least once on the output of the elementary circuit i.

However, the structure of many one-pulse networks does not ensure these conditions to be satisfied. The checking circuit should then be modified.

Namely, if the condition a/ is not satisfied then, instead of one and-gate for the elementary circuit i, more and-gates of the type /5/ should be applied for the elementary circuits chosen so that the sum of their output states would sufficiently often equal 1.

If condition b/ is not satisfied, then two-argument and-gates should be adjoined to the checking circuit for all such pairs of elementary circuits i, j, for which there exists an elementary circuit k /not necessarily different from i or j/ such that $c_{ik}\, c_{jk} = 1$.

If, for instance, $\sum_{l=1}^{N} a_l^\tau = 2$, $a_i^\tau = 1$, $a_j^\tau = 1$

and if $b_{ik}^\tau\, c_{ik} = 1$, $b_{jk}^\tau\, c_{jk} = 1$

then there is $\sum_{l=1}^{N} a_l^\tau = 2$, $\sum_{l=1}^{N} a_l^{\tau+1} = 1$

during a correct network operation. In this case the and-gate of elementary circuit outputs i, j detects for the moment τ an erroneous state of the network $\left(\sum_{l=1}^{N} a_l^\tau = 2\right)$ which for the moment $\tau + 1$ cannot be detected $\left(\sum_{l=1}^{N} a_l^{\tau+1} = 1\right)$.

Thus, the checking circuit of the method of delayed error detecting consists of:

a/ or-gate and its negation for detecting the absence of "ones" in the network,

b/ several circuits, every one of which is a two-argument and-gate of an appriopriate elementary cirouit and an or-gate of the remaining elementary circuits. The criterion for selecting these chosen elementary circuits and for their number is the obtaining of the sum of their output states being sufficiently often equal to 1.

c/ the and-gates of all pairs of the outputs of elementary circuits i, j for which there exists such an elementary circuit k that $c_{ik} c_{jk} = 1$,

d/ the or-gate of the circuit outputs mentioned in points a/, b/, c/.

In this method, contrary to the methods of the previous chapter, the error signalization does not appear directly after an error delay depending only on the checking circuit operation time, but after an error delay conditioned by the structure of the network, the place and the time of the appearance of the error. Namely, if in the checked network a second "one" appears, the error will be detected when at least one of the "ones" will reach one of the selected elementary circuits, mentioned in point b/, or both "ones" will reach any of the pairs of elementary circuits, mentioned in point c/.

The method of a delayed error detection described in this chapter had been used for checking the central control network, as well as for checking networks controlling the performance of arithmetic operations in the ZAM-3 computer constructed at the Institute of Mathematical Machines in Warsaw.

4. CONCLUSIONS

From a practical viewpoint, according to notes in chapter 2, interesting checking circuits are only those which are small /as compared with the checked network/ and appropriately efficient.

Out of the given methods the following can be taken into account:
a/ method 4 chapter 2, which is a simplification of method 3, b/ eventually other modifications of method 3 not being discussed in the present paper, c/ the method of a delayed error detection given in chapter 3.

The method 3 chapter 2, especially its modifications /for example method 4 chapter 2/ are suitable to check a network based on a technique, for which the greatest possibility of error appearing is during the change of the zero-one states of elementary circuits. The method chapter 3 /method of delayed error detecting/ does not need this assumption.

The above discussed methods may be used not only to one-pulse networks. They also may be applied to networks that differ from one-pulse networks, by some of outputs of elementary circuits not being connected with the inputs of other elementary circuits of the considered network. Then, the network has not the properties /2//ref. to chapt. 1/. Such a network may be easily complemented so as to obtain a one-pulse network, for which the above-mentioned checking methods are valid. For this purpose it is sufficient to connect the outputs of elementary circuits, not being connected with any inputs, with the inputs of an additional storing elementary circuit that is adjoined to the network. It may be formally accepted, that the adjoined elementary circuit is the checking circuit part, and does not change the network itself. Practically, the adjoining of such an elementary circuit in order to get a one-pulse network is not necessary in the majority of cases, especially if one resigns from sygnalizing an erroneous zero-state of the network, /i.e. for $\sum_{i=1}^{N} a_i^t = 0$/.

The above consideration is a formal basis for using the discussed methods for certain not one-pulse networks as well.

It is worth adding that an arbitrary segment of a one-pulse network may always be changed into a one-pulse network by adjoinning one storing elementary circuit.

Obviously, the described methods of checking can also be used for one-pulse parts of not one-pulse networks. It does not require any argumentation.

5. EXAMPLES OF CHECKING THE NETWORK OPERATION.

Example 1. The method of detecting two "ones" on the outputs of two directly connected elementary circuits /method 4, chapt. 2/.

In scheme 1 a network is presented that is a segment of a one-pulse network. The network scheme is simplified. Elementary circuits performing boolean "sums of products" /1/ are shown in the form of triangles. The connections of outputs of circuits outside the network with the inputs of the network elementary circuits /see factors b_{ij}^t /1// are omitted in the soheme. The influence of the omitted connections /b_{ij}^t states/ on the network operation is taken into account, if it is assumed that at every moment T strictly one connection takes the state 1 between the output of every elementary circuit and one input of the network elementary circuit or one of the output points B, C, D. Near the network scheme another one is given of one elementary circuit in which and-gates, or-gates and the delay line T are each shown separately. If at the moment τ, there occures a "one" on the output of the elementary circuit i, and a connection exists between the elementary circuits i and j as also $b_{ij}^{\tau} = 1$, then at the moment $\tau + 1$ a "one" will appear on the output of the elementary circuit j.

In other words the network can be treated as a set of T delay lines connected in such a way that they may be on or off /$b_{ij}^t = 1$ or $b_{ij}^t = 0$/ so that on the output of every elementary circuit strictly one connection is on at every moment.

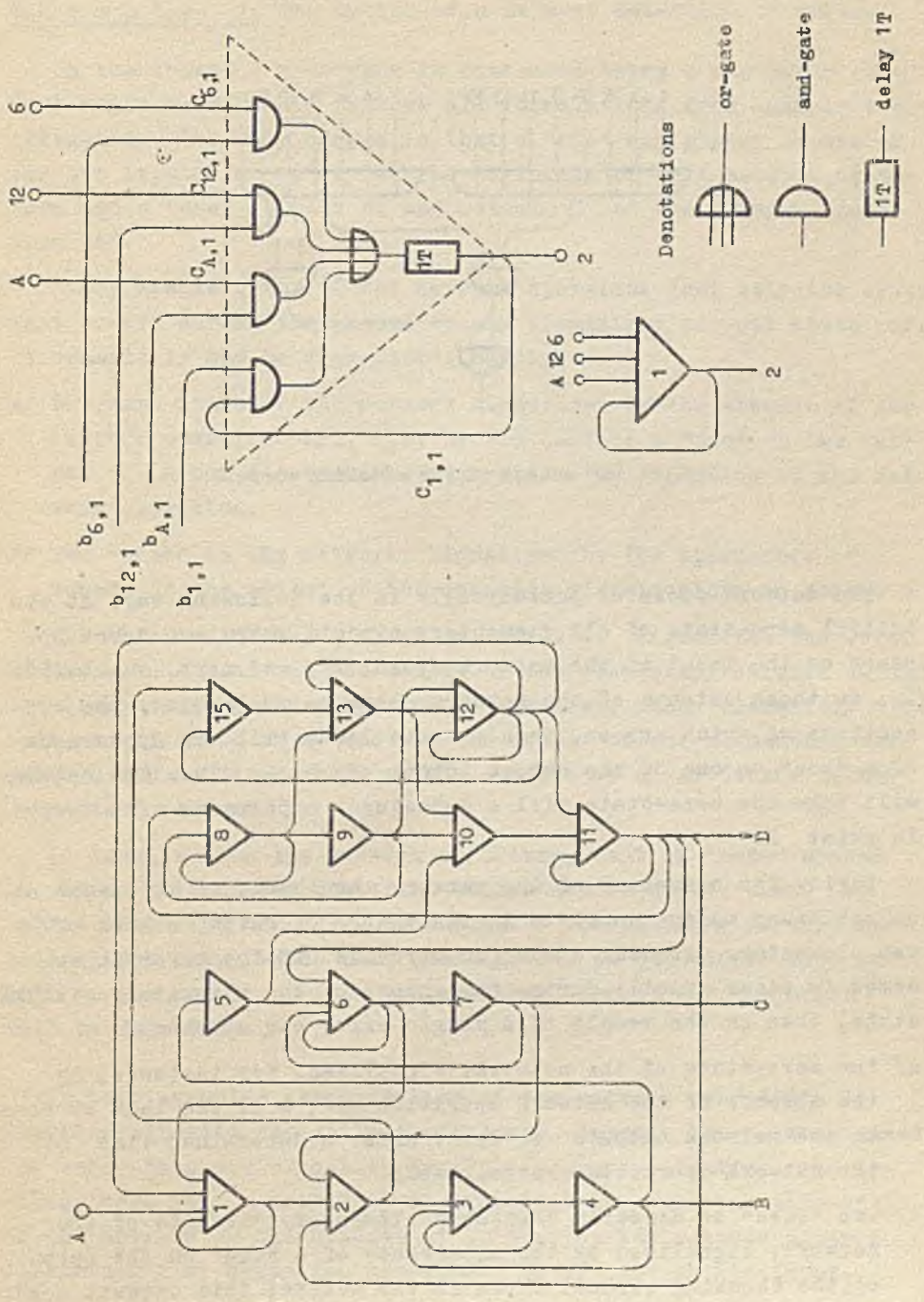

Fig. 1. The scheme of a checked network and the scheme of the elementary circuit of the checked network.

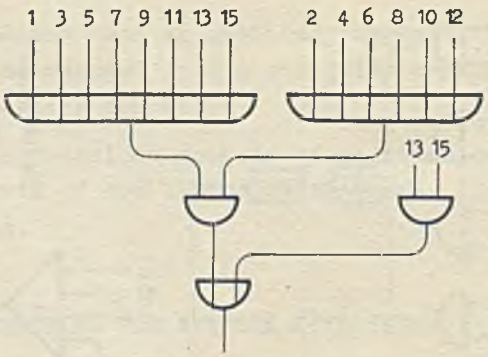

Fig. 2. The scheme of the checking circuit.

The network operates periodically in the following way. At the initial zero-state of all elementary circuit outputs a "one" appears on the input of the network /point A/, and next, successively, on those outputs of the network elementary circuits, the connections of which are on. Such a state lasts till the appearance of a "one" on one of the output points B, C, D. Then the network will take the zero-state till a subsequent appearance of a "one" in point A.

During the operation of the network the change of its state at an arbitrary moment consists in the change of output states of two elementary directly connected circuits. If the error is assumed to occur usually during the change of the elementary circuit state, then as the result of a single error one obtains:

a/ the zero-state of the network, signalized, for instance, by the absence of the network operation end, i.e. the lack of "one" on the network outputs B, C, D, after a determined time of the network operation, respectively

b/ two "ones" on directly connected elementary circuits of the network, signalized by the appearance of a "one" on the output of the checking circuit shown in the scheme; this circuit needs no description because of its simplicity.

The scheme of the checking circuit is shown in scheme 2.

E x a m p l e 2. The method of a delayed detection of error.

In the scheme 3 a network is presented being a one-pulse network segment. For this network all formulations from example 1 are obligatory. The only change is that a "one" may appear on one of the two inputs A or B at the beginning of this network operation and a "one" appears on one output C at the network operation end.

Every single error of the network operation /not only the error that occurs during the change of any elementary circuit state ref. to example 1/ may be signalized, namely:

a/ the zero-state of the network signalized by the absence of the network operation end, i.e. by the lack of a "one" on the output C after a determined time since the beginning of the network operation,

b/ two "ones" in the network, signalized by the appearance of a "one", on the output of the checking circuit shown in scheme 4

The checking circuit, shown in scheme 4, signalizes the error if there is a "one" on the output of the elementary circuit 4, and simultaneously on the output of an arbitrary other elementary circuit, or if there is a "one" on the output of the elementary circuit 7, and simultaneously on the output of an arbitrary other elementary circuit.

It results from the network structure, that if "ones" appear on the outputs of two arbitrary elementary circuits, then, at latest after the time 7 T, /the time of the checking circuit operation not being taken into account/ one of the "ones" will appear on the output of 4 or 7 elementary circuit and the error will be detected.

In both examples the detection of the network zero-state in checking circuits has not been foreseen, because the network takes the zero-state periodically, during a correct operation, and because there is a possibility to signalize an erroneous zero-state of the network by the absence of a "one" on its outputs after a determined time since the appearance of a "one" on its input.

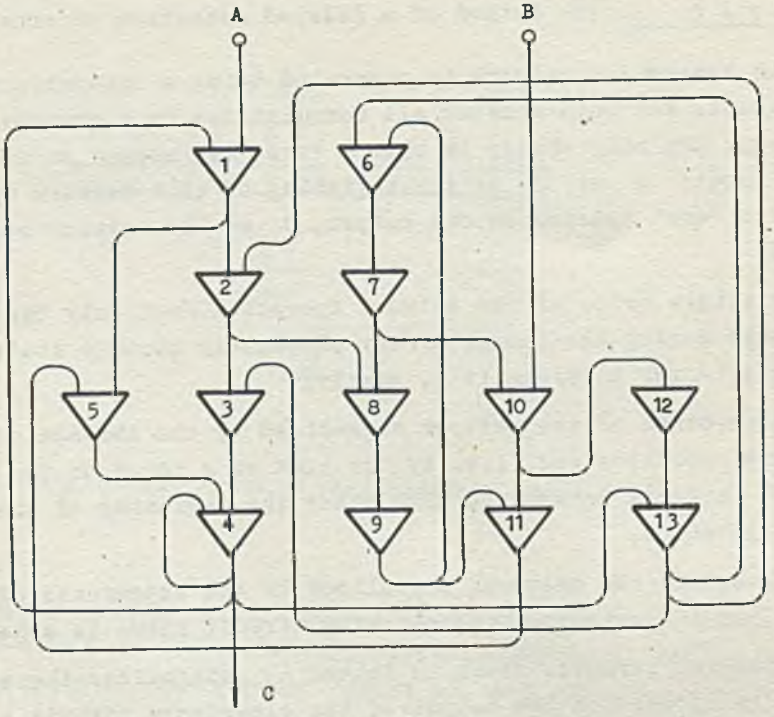

Fig. 3. The scheme of the checked network.

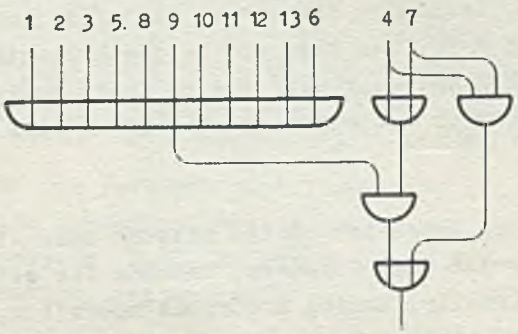

Fig. 4. The scheme of the checking circuit.

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