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The paper concerns the parity check of arithmetic operations in digital computers. The check methods presented in other papers, dealing with this problem, discuss the parity of a total sum of digits of arguments, of the operation result and of the carries occurring during the operation. In this paper attention is drawn to the fact that every error of a carry occurring during the operation changes its result, so that a summarized error becomes undetectable in case of an additional carry circuit not being applied in check circuits. The analysis of the carry error is presented in an example of the addition of binary numbers.

In papers [4] and [5] methods of circuit checking of arithmetic operations were discussed. These methods are based on dependence appearing between the digits of arguments, digits of results of the arithmetic operations and values of carries occurring during the operation. The parity check of arithmetic operations is a particular case of the modular weight check described in the above-mentioned papers. It detects all such errors in which the total number of erroneous digits and carries, appearing during the operation, is odd. The purpose of this paper is to show that the above formulation does not permit to draw a conslusion about the detection of every single error occurring during an arithmetic operation. It results, therefore, that every error of a carry causes such a change of the operation result that the summarized error becomes undetectable in case an additional carry circuit is not applied. This additional carry circuit may be treated as a part of the check circuit.

The analysis of the carry errors is presented in an example of the addition of binary numbers. In order to simplify the considerations we shall consider only the addition of absolute values of numbers

$$a = \sum_{i=0}^{N} a_i 2^i \tag{1}$$

$$b = \sum_{i=0}^{N} b_i 2^i \tag{2}$$

the sum of which is

$$s = \sum_{i=0}^{N} s_i 2^i \tag{3}$$

where a_i, b_i, s_i take values 0 and 1.

Values of s_i bits are determined by the recurrent formula

$$a_i + b_i + c_i = s_i + 2\, c_{i+1} \tag{4}$$

where the carry c_i takes values 0 and 1.

Assuming $c_0 = 0$ we obtain from /4/ the values s_i and c_{i+1} for $i = 0, 1, \ldots, N$. From the assumption that the formula /3/ defines the sum s we obtain $c_{N+1} = 0$. /The assumptions $c_0 = 0$ and $c_{N+1} = 0$ have been accepted only to shorten the considerations/.

When summing up the sides of the equation /4/ for i from 0 to N we obtain

$$\sum_{i=0}^{N} a_i + \sum_{i=0}^{N} b_i + \sum_{i=0}^{N} c_i = \sum_{i=0}^{N} s_i + 2 \sum_{i=0}^{N} c_{i+1} \tag{5}$$

and, hence, for $c_0 = 0$ and $c_{N+1} = 0$ we have

$$\sum_{i=0}^{N} a_i + \sum_{i=0}^{N} b_i = \sum_{i=0}^{N} s_i + \sum_{i=0}^{N} c_i \qquad /6/$$

From /6/ results the modular equation

$$\left(\sum_{i=0}^{N} a_i + \sum_{i=0}^{N} b_i + \sum_{i=0}^{N} s_i + \sum_{i=0}^{N} c_i\right) \text{Mod } 2 = 0 \qquad /7/$$

This equation is a particular case of the modular equation /37/ from [4] page 36. This also results from the equation /24/, paper [5] page 56. The appearance of pluses in parentheses on the left side of the equation /7/ instead of minuses is of no significance in Mod 2. The equation /7/ is the basic formula for the parity chec of addition.

We shall assume that all the values a_i, b_i, s_i, c_i $(i=0,1,\dots,N)$ may be checked, and that there exists in the computer a check circuit checking the formula /7/.

Let us assume that during the addition a carry error occurs and the erroneous carry c_j' appears instead of the carry c_j $(c_j' \neq c_j)$, where $0 < j \leq N$.

Then, the equation

$$a_i + b_i + c_i = s_i + 2\, c_{i+1} \qquad \text{for} \qquad i = 0, 1, \dots, j-2 \qquad /8/$$

does not change and instead of the equation

$$a_{j-1} + b_{j-1} + c_{j-1} = s_{j-1} + 2\, c_j \qquad /9/$$

we obtain

$$a_{j-1} + b_{j-1} + c_{j-1} \neq s_{j-1} + 2\, c_j' \qquad /10/$$

and for $i = j, j+1, \ldots, N$ we obtain the equation

$$a_i + b_i + c_i' = s_i' + 2\, c_{i+1}' \qquad /11/$$

where values s_i' and c_{i+1}' are assigned recourrently for consecutive integers i. To simplify the considerations we assume $c_{N+1}' = 0$. This assumption is of no importance for the results of considerations.

The difference between the right sides /9/ and /10/ is $+2$ or -2, due to which we obtain instead of /6/ the formula

$$\sum_{i=0}^{N} a_i + \sum_{i=0}^{N} b_i \neq \sum_{i=0}^{j-1} s_i + \sum_{i=j}^{N} s_i' + \sum_{i=0}^{j-1} c_i + \sum_{i=j}^{N} c_i' \qquad /12/$$

where the difference between the left and right side is also $+2$ or -2. Because this difference is even, we obtain, instead of /7/, the following equation

$$\left(\sum_{i=0}^{N} a_i + \sum_{i=0}^{N} b_i + \sum_{i=0}^{j-1} s_i + \sum_{i=j}^{N} s_i' + \sum_{i=0}^{j-1} c_i + \sum_{i=j}^{N} c_j' \right) \operatorname{Mod} 2 = 0 \qquad /13/$$

It results from /7/ and /13/ that the parity check circuit of the sum of digits of numbers a, b, s and of carries $c_0, c_1, \ldots, c_N$ does not detect the change of the carry c_j into the erroneous carry c_j'. The conclusion may be drawn that such a circuit does not detect errors in the carry circuit of an adder. However, it detects every odd number of all other erroneous bits occurring in the adder.

In order to detect every odd number of errors appearing in an adder, another independent carry circuit should be adjoined to the adder. The inputs of the above carry circuit should be connected parallel with those of the proper carry circuit of the adder. The outputs of the additional carry circuit should be joined only to the check circuit.

In such a solution the check circuit checks the states a_i, b_i, $s_i (i = 0,1,\dots,N)$ of the adder, and the states $c_i (i = 0,1,\dots,N)$ of the additional carry circuit. The check circuit, based on modular equation /7/ signalizes the appearance of every odd number of errors in the adder /including errors appearing in the carry circuit/. Such a solution was applied in the ZAM 3 computer at the Institute of Mathematical Machines in Warsaw.

In an analogous way it may be easily proved that in the case of subtraction, multiplication and division, the parity check circuit without an additional carry circuit does not detect any carry errors.

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