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## MODEL OF COMMUTATION FOR POWER ELECTRONIC CONVERTER

Summary. The paper presents model of commutation of power electronic converter. It is a piecewise linear model based on piecewise model of the switch (diode). It is described basing on circuit theory, geometry and linear algebra. The model is the part of generalised model of power electronic converter that encompasses its dynamics that is represented by means of two-dimensional directed node graph. The theory is illustrated with examples.

## MODEL KOMUTACJI PRZEKSZTAŁTNIKA ENERGOELEKTRONICZNEGO

Streszczenie. W artykule przedstawiono model komutacji przeksztaltnika energoelektronicznego. Jest to model odcinkami liniowy, bazujacy na modelu odcinkowo liniowym zaworu (diody). Opis oparty jest na teorii obwodów, geometrii oraz algebrze liniowej. Model komutacji jest częścią modelu uogólnionego przekształtnika energoelektronicznego, który zawiera model dynamiki reprezentowanej w postaci dwuwymiarowego grafu skierowanego. Teoria została zilustrowana przykładami.

## 1. INTRODUCTION

Power electronics still develops new converters and systems that are indispensable for contemporary technology. In order to study and design these systems it is necessary to have enhanced models of power electronic converters (PEC). The extensive literature on the models of PEC, e.g., $[1,2,6,7,9]$ is not concentrate on commutation of PEC. The commutation in PEC has to be regarded important, especially when the dynamics of PEC is considered.

The paper is devoted to the piecewise model (PL) of the commutation of the PEC.
Essentially the paper is based on the [3] where PL model of the commutation was studied. The model of the commutation has to be treated as an integral part of the model of PEC that allows the analysis its of dynamics. Existing literature on power electronics do not report works that are focussed on PL models of commutation in PEC.

The connection of the model of commutation with qualitative analysis of the dynamics of PEC [8] is shortly discussed in the paper. This method of analysis of PEC dynamics is also termed as equivalent circuit-to-equivalent circuit analysis [12].

The model of commutation is described in categories of electrical circuit and also in terms of geometry and linear algebra. The model of commutation is embedded in state space and is valid for arbitrary dimensions. The switches in the model can be diodes as well as controlled switches. Such model related to PEC has not been presented in literature yet, except [3].

Some questions that came up during the investigations of power electronics were primary inspiration to undertake the thorough study of model of PEC. These questions are worth
mentioning here. They are: How many equivalent circuits can be observed in the course of the operation of 3-phase diode bridge converter supplied from 3-phase voltage source where current source is the load on DC side. Is it $6,12,32,64$ or something different? Is the sequence of these equivalent circuits unique? What parameters of the converter influence the number of equivalent circuits and its sequence? The answers can be found basing the proposed model.

## 2. MOTIVATION. AIM OF THE WORK. ASUMPTIONS

The need for efficient and thorough model of PEC (and the model of commutation in it) motivates the work presented in this paper. The model allows finding answer for some not obvious questions. It is the firm background for analysis of PEC that includes its dynamics.

The description of the PL model of commutation of PEC together with the discussion of the overall model of PEC that encompasses the equivalent circuit-to-equivalent circuit dynamics is the aim of the paper [12].

The following assumptions have been taken: i) The model of the commutation (structure of commutation) is confined to diode converters. ii) The diode model is PL one (the diode is termed perfect diode, cf. section 5. iii) The model of PEC is also PL type, termed perfect converter. iv) Capacitors and inductors are linear.

## 3. MODEL OF PEC

### 3.1. Models of switch

The models of switches are PL resistive. They are called perfect switches. There are two basic types of switches distinguished: i) uncontrolled - diodes and ii) controlled - transistors (or thyristors). The diode (perfect diode) is described by (3.1) and its $u-i$ characteristic is in fig. 3.1a. It is one-port piecewise linear resistance. The characteristic $u-i$ has two branches: i) reverse biasing ( $R$ ) and ii) conducting ( $F$ ), represented by state of diode, $n_{\mathrm{D}}=0$ and $n_{\mathrm{D}}=1$ respectively.

$$
R_{D}=\left\{\begin{array}{l}
R_{R} \Leftrightarrow-u>0 ; R ; n_{D}=0  \tag{3.1}\\
R_{F} \Leftrightarrow i \geq 0 ; F ; n_{D}=1
\end{array}\right.
$$

Fig. 3.1. $u-i$ characteristic of diode (a) and transistor (b)
Rys. 3.1. Charakterystyka napięciowo-pradowa diody (a) oraz tranzystora (b)
The transistor (perfect transistor) is described similarly, cf. $u-i$ characteristic in fig. 3.1b. It is one-port piecewise linear resistance with the $u-i$ characteristic with three branches: $(R)$ - reverse biasing, $(F)$ - conducting and $(B)$ - blocking.

### 3.2. PEC model

There are two basic types of PEC models. The first one is of invariable topology (ITM). The second one is termed the model of variable topology model (VTM). Their Kirchhoff equations are invariable or variable respectively.

The ITM model is described by the equations (3.2). The model is allowed to contain perfect as well as ideal switches and exists under condition that the switches in $e-C-S$ circuits and $j-L-S$ cut-sets are perfect ones not ideal. Each commutation changes the resistance of switch/switches. The model can be represented as a set of equivalent circuits with its time sequence for given dynamics and control.

$$
\begin{array}{ll}
\frac{d x}{d t}=A_{1} x+A_{2} y_{O}+B_{1} u+B_{2} \frac{d u}{d t}, & x=\left[\begin{array}{ll}
u_{a} & i_{L L}
\end{array}\right]^{T}, y_{O}=\left[\begin{array}{ll}
u_{v t} & i_{v}
\end{array}\right]^{T}, \\
y_{I}=C_{1} x+C_{2} y_{O}+D_{1} u+D_{2} \frac{d u}{d t}, & y_{I}=\left[\begin{array}{ll}
i_{v t} & u_{v 1}
\end{array}\right]^{T}, u=\left[\begin{array}{ll}
u_{e} & i_{j}
\end{array}\right]^{T,}  \tag{3.2}\\
y_{O}=N(s v) y_{I}, & \\
s v=f\left(y_{I}, y_{o}, g\right), &
\end{array}
$$

where $t$ - tree branches, $l$-link branches, $v$-switch branches, $s \nu$-state of switches.
The second type of PEC model - VTM differs from ITM because its switches and Kirchhoff equations. Switches here can be exclusively ideal ones if. The commutation needs the change of Kirchhoff equations. Similarly, this model can be presented as a set of equivalent circuits together with its time sequence.

## 4. COMMUTATION

Commutation can be described as the process of switching off-on-off-on-... , taking place in electric circuits/systems. Although many different types of commutation are defined in power electronics, e.g., $[6,7]$ this paper concentrates on the most general idea of the commutation basing on piecewise linear description - (PL description).

The commutation is usually associated with dynamics but the thorough investigation of this process demonstrates that commutation can also be treated as a static notion. In the first part of this paper the commutation process is described by means a commutation structure that is a static object. But when the dynamics is imposed the resulting can change according to the dynamics.

It is obvious that the commutation can be analysed numerically (for instance PSPICE) but the results are partial ones, being valid for given numerical data, not embracing all possibilities.

## 5. COMMUTATION STRUCTURE

The commutation structure CS describes the whole commutation in the piecewise model, PL, of PEC. The schematic diagram of $C S$ is depicted in fig. 5.1. The commutation structure is formulated here as the set of three substructures: i) hypothetical commutation (sub)structure $H S$, ii) basic commutation (sub)structure $B S$ and iii) feasible commutation (sub)structure $F S$. They are related with each other due to formula: $C S:=F S \subseteq F B \subseteq F H$, where $F S=\{F S i\}$. does not lead to a mistake. Each of them are characterized in the subsequent part of this section as a set of relevant objects. Further in the paper the substructures are called structures in case it is not misleading.


Fig. 5.1. Commutation structure - $C S$
Rys. 5.1. Struktura komutacji - CS

### 5.1. Hypothetical commutation structure - HS

The hypothetical commutation structure $H S$ is the set of equivalent circuit with its hypothetical time sequence. The number of equivalent circuits in this structure depends on the number of the switches in PEC. The time sequence is arbitrary and is determined by the easiness of relevant calculations, for example could be given by binary code where each entry is given by state of diodes $s_{\mathrm{DD} i}=i \mid i=1 \ldots 2^{\mathrm{nD}} ; 2^{\mathrm{nD}}=n_{H} ; n_{\mathrm{D}}-$ number of diodes in PEC.

Each equivalent circuit $i$ is defined by the set of $n_{\mathrm{D}}$ homogeneous linear inequalities (5.1) or (5.2) where diode number is indicated by variable $N_{\mathrm{D} j}=\left.j\right|_{j=1} \ldots n_{\mathrm{D}} ; j$ is also the number of linear inequality connected with given diode.

$$
\begin{align*}
& -u_{i j}=A_{11 i j} e+A_{12 i j} j>0,  \tag{5.1}\\
& i_{i j}=A_{2 i i j} e+A_{212 i j} j \geq 0 . \tag{5.2}
\end{align*}
$$

The $H S$ for PEC with controlled switches is given similarly.
When the number of equivalent circuits is taken into consideration $H S$ is the largest structure.

The algorithm of setting inequalities (5.1), (5.2):

1. Replace of $C$ and $L$ with voltage and current sources respectively. (It results in global equivalent circuit that contains only voltage and current sources and resistors (diodes are PL resistors)).
2. Set the equations for the global equivalent circuit.
3. Resolve the set of circuit equations for the voltage across the diodes and diode currents.
4. For each state of diodes $s_{D D}$.
4.1. Set resistance of the diode, $R_{D}=R_{R}$ for reverse biased diodes and $R=R_{\mathrm{F}}$ for the conducting diodes.
4.2. Set inequality for each diode: $-u>0$ when it is reverse biased and $i \geq 0$ for the diode that is to conduct. There are set of $2^{n}$ Dets of $n_{D}$ inequalities is the result.

### 5.2. Basic commutation structure - $B S$

The basic commutation structure is embedded in $n_{\mathrm{S}}$-dimensional state space. It is defined by the sets of inequalities (5.1), (5.2). Each inequality is defined by corresponding linear homogeneous equation which in turn defines hyperplane ( $H$-plane) and convex halfspace. The set of halfspaces cuts in $n_{\mathrm{S}}$ space the convex polyhedra cones of dimensions $C^{\mathrm{n}}{ }_{\mathrm{S}}, C^{\mathrm{n}}{ }_{\mathrm{S}-1}$, $C^{\mathrm{n}}{ }_{\mathrm{s}-2}, \ldots, C_{1}, C_{0}$. The analysis of the conversion process has to be limited to the certain region of the state space. The limits are imposed by the physics of the systems. It means that each state is enclosed within global boundary: $x_{\min } \leq x \leq x_{\max }$. The boundaries form a global convex polytope in $n_{\mathrm{S}}$ space.

Apart of the geometrical interpretation of basic commutation structure two other exist. The first is algebraic one. The second interpretation comes from description of PEC as electrical circuit (cf. (5.1), (5.2)).
Eventually the basic commutation structure can be derived from the $2^{\mathrm{n}}{ }_{\mathrm{D}}$ solutions of $n_{\mathrm{D}}$ sets of inequalities $[8,13,3]$. These solutions, expressed in geometry terms, should be stored as a certain ordered data [8, 13]. It is so because this data is needed in the analysis of the dynamics of the converter [8,10, 11]. As an example of the data that has to be stored and handled is the adjacency, where $n \mathrm{~S}$-cone is adjacent to the neighbour $n \mathrm{~S}$-cone sharing ( $\mathrm{nS}-1$ ), ( $\mathrm{nS}-2$ ) ... faces. The geometrical model is connected directly with algebraic one and with the circuit model of PEC (c.f. (5.1), (5.2)).

It is possible to establish maximal number of basic equivalent circuits and it results in formula (5.3) and table 5.1.

$$
n_{B}\left(n_{D}, n_{S}\right)=\left\{\begin{array}{cc}
2^{n_{D}} & : n_{D} \leq n_{S}  \tag{5.3}\\
\sum_{i=1}^{n_{S}-1} \frac{\left(n_{D}-2-i\right)!}{\left(n_{D}-n_{S}-1\right)!\left(n_{S}-i-1\right)!} 2^{(i+1)} & : n_{D}>n_{S}
\end{array}\right.
$$

Table 5.1
Maximum number of basic equivalent circuits $n_{B}$

|  |  | $n_{p}$ |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 2 | 3 | 4 | 5 |  |  |
| $n_{S}$ | 1 | 2 | 2 | 2 | 2 | 2 |  |
|  | 2 | 2 | 4 | 6 | 8 | 10 |  |
|  | 3 | 2 | 4 | 8 | 14 | 22 |  |
|  | 4 | 2 | 4 | 8 | 16 | 30 |  |
|  | 5 | 2 | 4 | 8 | 16 | 32 |  |

The formula (5.3) can be derived using geometry or/and linear algebra. It can be proved basing on induction reasoning. It is necessary to do it separately for two conditions: i) $n_{D} \leq n_{\mathrm{S}}$ and ii) $n_{\mathrm{D}}>n_{\mathrm{S}}$. Geometrical approach consists in introducing to the state space the hyperplanes that is given by the voltage across diodes, $u_{i}=0$. The first part of reasoning concerns $n_{\mathrm{D}} \leq n_{\mathrm{s}}$. The first $H$-plane is given by the voltage across the diode $u_{I}=0$. This $H$-plane divides the space into two regions. Each one corresponds to the equivalent circuit. Next, the second hyperplane $u_{2}=0$ is introduced. This new $H$-plane divide each of existing regions of the state space into two resulting in double number of regions in comparison with the first case. In order to find the number of basic equivalent circuits for any $n_{\mathrm{S}}$ and $n_{\mathrm{D}}$ one introduce ( $n_{\mathrm{D}}+1$ ) hyperplane in $n_{\mathrm{S}}$. It means that the new hyperplane given by $\left(n_{\mathrm{D}}+1\right)$ diode has dimension $\mathbf{n}_{\mathbf{S}}-1$
and is divided by ( $n_{\mathrm{D}}-1$ ) hyperplanes given by already existing diodes of dimension ( $n_{\mathrm{S}^{-}}$). This results in number of regions of this hyperplane that is equal $n_{\mathrm{B}}\left(\left(n_{\mathrm{S}}-1\right),\left(n_{\mathrm{D}}-1\right)\right)$. Each region of this $\left(n_{\mathrm{D}}+1\right)$ hyperplane is the ( $\left.n_{\mathrm{S}^{-}} 1\right)$-facet of the region of $n_{\mathrm{S}}$ dimension. It gives $n_{\mathrm{B}}=n_{\mathrm{B}}\left(\left(n_{\mathrm{S}^{-}}\right)\right.$, $\left.\left(n_{\mathrm{D}}-1\right)\right)+n_{\mathrm{B}}\left(\left(n_{\mathrm{S}}\right),\left(n_{\mathrm{D}}-1\right)\right)$. The formula (5.3) can be also obtained using linear homogeneous equations.

### 5.3. Feasible commutation structure - FS

The feasible commutation structure is the part of the basic commutation structure. It is defined by actual dynamics of PEC. Applying the notion of dynamics, the orbit of the flow one can state that for different dynamics or at least for different initial condition the different orbit exists. Therefore given orbit passes by certain set of regions (convex cones) of the state space, where each of them corresponds with an equivalent circuit. Some details of the feasible structure are illustrated in example 5.1 and discussed in section 6.

Example 5.1: 4-diode bridge rectifier
The example is used for explanation aforementioned ideas. The schematic diagram of the rectifier is depicted in fig. 5.2. The characteristic of $u-i$ of the diode is in fig. 3.1a.



Fig. 5.2. 4-diode bridge rectifier (example 5.1)
Rys. 5.2. Mostkowy prostownik czterodiodowy (przykład 5.1)

Fig. 5.3. Basic commutation structure $B S$ (different resistance of diodes $R_{\mathrm{R}} / R_{\mathrm{F}}:=D 1: 10 \Omega / 2 \Omega ; D 2: 11 \Omega / 1 \Omega ; D 3: 12 \Omega$ $2,5 \Omega, D 4: 13 \Omega / 0,5 \Omega$ ); notation: conducting $=1$, reverse biasing $=0$
Rys. 5.3. Podstawowa struktura komutacji $B S$
The converter is supplied from voltage source $e$ and is loaded by current source $j$. The hypothetical commutation structure $H S$ is formed by $2^{n}{ }^{n}=2^{4}=16$ equivalent circuits. In case each diode has different resistance the resultant basic commutation structure is as in fig. 5.3. It is obtained due to algorithm described in 5.2. For example for state of diodes $s_{\mathrm{DD}}=1101$ the region in $e-j$ plane is given as a solution of the following set of inequalities: $i_{1}>0, i_{2}>0,-u_{3} \geq 0$, $i_{4}>0$. There are 8 regions of 2D (2-dimension) within which the voltage $e$ and current $j$ are only constrained by the commutation lines. Other 8 regions are of 0 D being reduced to the origin. For points ( $e, j$ ) lying on the commutation line, for instance, on line: 1111/1101 all diodes are in neutral state $N$ (fig. 3.1). When the resistances of diodes are equal the basic commutation structure consists of only 4 regions of 2D. In this case 8 regions are reduced to regions of 1D (commutation lines) and the remaining 4 to region of 0 D (the origin). The regions are called also cones.


Fig. 5.4. Basic commutation structure $B S$ and feasible commutation structure $F S$ (different resistance of diodes $R_{R} / R_{F}$ - fig. 5.3); trajectories: ABCDEF $\mathrm{GH} e=1 \sin (\omega \mathrm{t}), j=1 \cos (\omega \mathrm{t}) ; \mathrm{IJ}-e=1,2 \sin (\omega \mathrm{t}), e=$ $1,2 \sin (\omega \mathrm{t}), j=0,105 \sin (\omega \mathrm{t}) ; \mathrm{KL}-e=-1-0,2 \sin (\omega \mathrm{t})$, $j=1+0,2 \cdot \sin (\omega t)$
Rys. 5.4. Podstawowa struktura komutacji $B S$ i struktura osiagalna $F S$

To get feasible commutation structure it is necessary to impose concrete time functions on voltage source $e$ and current source $j$. There are three cases indicated in fig. 5.4: trajectory ABCDEFGH (circle), KL (segment on the commutation line 1111/0111) and IJ (segment that lays partially in the regions 0100 and 1001). In the real analysis the feasible commutation structure is defined by the dynamics of PEC. In presented example it is illustrated by replacement of current source $j$ by series $R-L$ circuit - fig. 5.5, 5.6. The dynamics is governed by differential equation solution of which is the trajectory in $e-j$ plane that in turn define the feasible commutation structure. In the presented example this feasible structure embraces 7 regions what means that one can observe 7 equivalent circuits.


Fig. 5.5. Basic commutation structure $B S$ and feasible commutation structure $F S$ (different resistance of diodes - fig. 5.3); load: series $R$ - $L$ circuit ( $R=1 \Omega, L=$ $=10 \mathrm{mH}, f=50 \mathrm{~Hz}$ )
Rys. 5.5. Podstawowa struktura komutacji $B S$ i struktura osiagalna $F S$


Fig. 5.6. Basic commutation structure $B S$ and feasible commutation structure $F S$ (resistance of diodes $R_{\mathrm{R}} / R_{\mathrm{F}}=10 \Omega / 1 \Omega$ ); load: series $R$ - $L$ circuit ( $R=1 \Omega, L=$ $=10 \mathrm{mH}, f=50 \mathrm{~Hz}$ )
Rys. 5.6. Podstawowa struktura komutacji $B S$ i struktura osiagalna $F S$

Example 5.2: 6-diode bridge rectifier
Schematic diagram of the rectifier is in fig. 5.7. It is supplied from AC 3-phase voltage source (equivalent to two line-to-line sources). The load, on DC side, is current source. The resistance of the diodes are different. The part of basic commutation structure is depicted in fig. 5.8. The hypothetical commutation structure embraces 64 equivalent circuits or 64 regions of 3 D . Basing on formula (5.3) or table 5.1 it is possible to arrive at the result of 32 regions that can be observed in fig. 5.8. The basic structure for more complex converters has to be analysed by means of computer - fig. 5.8 is the evidence.


Fig. 5.7. 6-diode bridge rectifier (example 5.2)
Rys. 5.7. Mostkowy prostownik sześciodiodowy (przykład 5.2)


Fig. 5.8. Basic commutation structure (BS) of 6 -diode bridge rectifier
Rys. 5.8. Podstawowa struktura komutacji $B S$ prostownika sześciodiodowego

## 6. REMARKS ON THE GLOBAL MODEL OF DYNAMICS OF PEC

The remarks on the PL dynamics of PEC are given here in short. The analysis of the global dynamics of PEC needs information concerning linear dynamics inside $n_{S}$ cones (related to equivalent circuits), dynamics on commutation $H$-planes and generalised dynamics embracing the state space that is placed inside global boundaries. The issue of dynamics is illustrated with example 6.1.

The analysis of the commutation can be split into three steps. The first is devoted to the local dynamics confined to each $n_{5}$ cone. The dynamics on commutation $H$-planes is analysed in the second step. The third step is the construction of global dynamics representation.

Local linear dynamics of each equivalent circuit is represented in $n_{S}$ cone with bundle of trajectories that start from $n_{\mathrm{S}}$ faces of given cone called $N$ faces and arrive at its $X$ faces [8]. The $N$ and $X$ faces are part of $n_{\mathrm{S}}$ faces of the $n_{\mathrm{S}}$ cone. The $N$ and $X$ faces correspond to the node of the local node graph. In other words, each $N$ face is projected through the cone in order to find which $n_{\mathrm{S}}$ face is obtained what means that $X$ face is defined. Thus $n_{\mathrm{S}}$ faces of the $n_{\mathrm{S}}$ cone of basic commutation structure are partitioned in this way. After that the connected directed node graph is constructed where each its node corresponds to $N$ face or $X$ face. The connections between nodes are directed from the node that represents $N$ face to the node given by $X$ face. The global directed node graph gives conservative description of the global dynamics of PEC [8].

Example 6.1: The dynamics of $\mathrm{AC} / \mathrm{DC}$ converter (fig. 6.1)
The dynamics is analysed and described in the form of directed node graph. It is supplied from AC voltage source $e=\mathrm{Esgn}(\sin 2 \pi \mathrm{ft})$. The converter has the following data: $f=50 \mathrm{~Hz}, R=10 \Omega$, $L=150 \mathrm{mH}, R_{\mathrm{R}}=10 \Omega, R_{\mathrm{F}}=1 \Omega$. The basic commutation structure is given in fig. 6.2. It consists 4 cones: $11,10,00,01$ indicated by 4 commutation lines: $D-O 0, K-O \mathrm{o}, M-O \mathrm{o}, B-O \mathrm{o}$. Two cones are divided by DC steady state lines: $F-O \mathrm{o}, S-O$ o. There are the arrows indicating the direction of the flow. The dynamics of PEC is mapped on the directed node graph - fig. 6.3. There are 4 types of nodes in it. The nodes drawn as double line circles belongs to global boundary ( $A B$, $B C, C D, D E, \ldots$ ). Next are the single line circles - they represent commutations that occur on


Fig. 6.1. AC/DC converter (example 6.1)
Rys. 6.1. Przeksztaltnik AC/DC (przykład 6.1)

Fig. 6.2. Partitioned basic commutation structure ( $B S$ ) (example 6.1)
Rys. 6.2. Podzielona podstawowa struktura komutacji (BS), (przykład 6.1)
$N / X$ lines (faces), e.g., $D-O_{0}$. The DC steady state is indicated by shadowed circles. There are two of them $-F-O_{0}, S-O_{0}$ in this case. They represent $X / X$ lines (faces). Two rectangulars with rounded corners $-\mathrm{C}-\mathrm{O}_{\mathrm{O}}$ and $L-\mathrm{O}_{\mathrm{O}}$ - are the map of commutation line that is crossed in state space when the voltage $e$ changes its sign. Single line directed connections show the flow direction between commutation lines and the lines of steady state; they are, for instance, $C D \rightarrow F O_{\mathrm{O}}, M O_{\mathrm{O}} \rightarrow S O_{\mathrm{O}}$. Double line arrows stand for switchings being generated by the voltage $e$. The sample of transient for $E=1 \mathrm{~V}$ and initial condition $i_{L}=5 \mathrm{~A}$, and 50 Hz is given in fig. 6.4. The steady state of which is $0,0215 \mathrm{~A}$ and $0,0535 \mathrm{~A}$.


Fig. 6.3. Directed connected graph representing global dynamics of PEC (example 6.1)
Rys. 6.3. Skierowany graf połaczeń reprezentujacy dynamikę PEC (przykład 6.1)


Fig. 6.4. Trajectory for $\mathrm{e}=1 \operatorname{sgn}(\sin (2 \pi \mathrm{ft}))$ (example 6.1)
Rys. 6.4. Trajektoria dla $\mathrm{e}=1 \operatorname{sgn}(\sin (2 \pi \mathrm{ft}))$ (przykład 6.1)

## 7. CONCLUSIONS

1. There is the piecewise linear (PL) model of commutation structure described in the paper. The model is based on homogeneous linear inequalities. It has been discussed in geometric terms derived form PEC circuit model.
2. The basic commutation structure $(B S)$ is unique. It encompasses all possible equivalent circuits. The model is embedded in $n S$-dimensional state space. It is invariable with respect to given state variables.
3. The described model of commutation is the important source of information about conversion process and the base for qualitative analysis of PEC dynamics.
4. The main advantage of the dynamics that is described in the form of connected directed graph is that it gives conservative picture of global dynamic.
5. The efficient usage of the described model requires its computer implementation. The adaptation of existing software, e.g., $[8,11,5]$, is could be the solution.
6. Continuation of the work should embrace PEC models with controlled switches that are supplied from AC sources.

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