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800 W, 16 MHz LABORATORY CLASS E INVERTER

Summary. The paper describes the design and performance of a high-efficient, 800 W, 16 MHz Class E inverter without an external shunt capacitor. The inverter is built employing a DE-SERIES MOSFET and a gate driver from Directed Energy, Inc. (DEI). Inverter design and inverter performance characteristics are presented and compared to the results obtained from SPICE simulation. A slightly different configuration, Class EF inverter, is analysed as an example of possibility for improvement of the Class E inverter performance.

LABORATORYJNY FALOWNIK KLASY E 800 W, 16 MHz

Streszczenie. W pracy przedstawiono opis konstrukcji i właściwości wysokoczęstotliwościowego falownika klasy E (800 W, 16 MHz) bez zewnętrznego kondensatora równoległego. W konstrukcji falownika wykorzystano tranzystor typu DE-SERIES MOSFET ze sterownikiem dedykowanym, oba firmy Directed Energy, Inc. (DEI). Wyniki pomiarów laboratoryjnych falownika zostały porównane z wynikami symulacji w programie SPICE. W celu poprawy właściwości falownika klasy E przeanalizowano jego zmodyfikowaną wersję, nazwaną falownikiem klasy EF.

1. MOTIVATION

The necessity of thorough (and experimental in it) examination of a Class E inverter without an external shunt capacitor, which operates at power level of 1 kW, frequency of 16 MHz and uses a DE-SERIES MOSFET, motivates this work.

2. INTRODUCTION

As the popularity of many high-frequency applications continues to grow, designers are forced to construct high-efficient, high-frequency power inverters. Class E inverters meet these requirements, e.g. 1 kW, 13,56 MHz, 88,6% - [7], 1 kW, 27,12 MHz, 74% - [3]. Additionally, their numerous advantages, such as high density of power processing, high reliability, simplicity, excellent designability, low cost and size, cause they are often used in industrial, scientific and medical applications. For example, they are applied in induction and dielectric heating, plasma generation, laser power supplies, glass and lens coating, transmitters for communications, portable light sources, DC/DC converters and medical implanted systems for power supply.

3. CLASS E OPERATION

Class E operation takes place when switching losses for one of the transistor transitions, on-to-off or off-to-on, are eliminated and for the other one are reduced. In other words, only one jump of current or voltage occurs during transistor switching.

Fig. 1a shows the most common Class E inverter configuration - [5, 8, 9]. The transistor is switched periodically. When the transistor is on, the drain-source voltage u_{DS} is low and a high drain current can flow. When the transistor is off, no current flows (excepting capacitive current), but a high drain voltage can exist. The capacitor C_1 (together with parasitic one) reduces switching losses during the on-to-off transition (ZVS+NZCS). The values of C_1, C_2, L_2, R, switching frequency f and duty ratio D are designed such that the drain-source voltage u_{DS} and the drain current i_D are zero during the off-to-on transition (ZVS+ZCS).

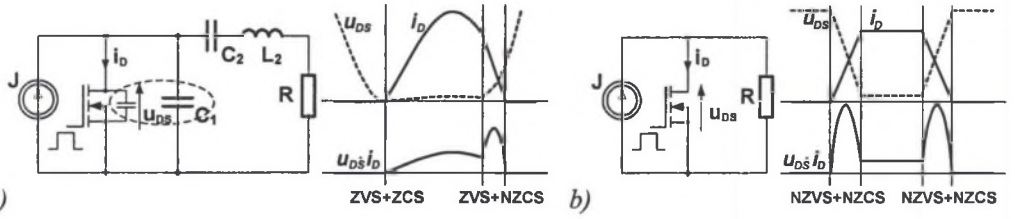

Fig. 1. Class E operation (a) vs. hard-switching (b)
Rys. 1. Porównanie pracy w klasie E (a) i twardego przełączania (b)

The different situation is for hard-switching - fig. 1b. The transistor voltage and current rise and fall with high speed during the off-to-on and on-to-off transitions (NZVS+NZCS). In a high frequency range switching losses dominate and significantly reduce efficiency.

4. ASSUMPTIONS

The following assumptions referring to the laboratory Class E inverter have been fixed:

- DC supply voltage of 220 V, output power of 1 kW and switching frequency of 16 MHz,
- a DE-SERIES MOSFET transistor as a switch with an ultrafast square-wave driver,
- elimination of the external shunt capacitor C_1 (fig. 1a),
- use of limited value of L_1 (fig. 2) to adjust Class E operation - [11].

DE-SERIES MOSFETs are transistors with low parasitic capacitances and inductances, isolated substrate, optimised for high speed switching - [1]. The single transistor of DE375-102N10A (1000 V, 10 A) with the square-wave driver of DEIC420 has been applied. The DEIC420 is a CMOS high speed, high current gate driver designed to drive MOSFETs in Class D and Class E applications. It can source and sink 20 A of peak current and produce voltage rise and fall times of a few nanoseconds.

Literature reports on building and testing Class E inverters employing DE-SERIES MOSFETs with square-wave drivers (1 kW, 13,56 MHz, 88,6% - [7], 1 kW, 13,56 MHz, 85% - [10]) and RF power MOSFETs from Advanced Power Technology (APT) with sine-wave drivers (500 W, 27,12 MHz, 83% - [2] and 1 kW, 27,12 MHz, 74% - [3]). Generally, sine-wave drive is more sophisticated and complex, e.g. an additional inverter is a part of it.

A construction of Class E inverter with the DE375-102N10A MOSFET driven by the DEIC420 gate driver has not been described in the literature yet. Moreover, it is quite a novelty to eliminate the external capacitor C_1 (fig. 1a) and use the inductance L_1 to adjust Class E operation of the inverter.

5. DESIGN CONSIDERATIONS

A MATLAB model of the Class E configuration has been used in the design of the inverter - fig. 2. The model includes on and off transistor resistances, finite DC-feed inductance L_1, finite output network $Q=\omega L_2/R$ and nonzero fall time of drain current during the on-to-off transistor transition. The design procedure is analogous to the one described in the paper [12].

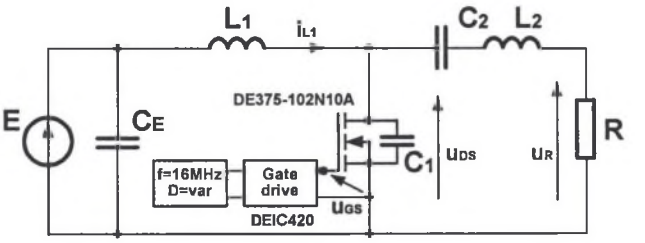

Fig. 2. Class E inverter schematic
Rys. 2. Schemat falownika klasy E

The schematic diagram is shown in fig. 2 and a view of the entire laboratory inverter in fig. 3. The notation in both figures is the same. The parameters of the inverter are as follows: C_E=100 nF (mica capacitors), L_1=9,1 μH (air-core inductor), C_1=160 pF (transistor parasitic capacitance), C_2=150 pF (mica capacitors with 1000 V rating), L_2=986 nH (946 nH - air-core inductor and 40 nH - parasitic inductance of load resistor), R=17 Ω (16,5 Ω - load resistor and 0,5 Ω - parasitic resistance of capacitor and inductor). These parameters have been measured using HP4294A Impedance Analyser at 16 MHz. The transistor and driver heatsink and the load resistor are cooled by means of water. The resistor is made up of 42 low-inductance resistors, 75 Ω each, connected in series and parallel (3x14). Fig. 4 illustrates a top view of the DE375-102N10A transistor and its DEIC420 driver with removed heatsink.

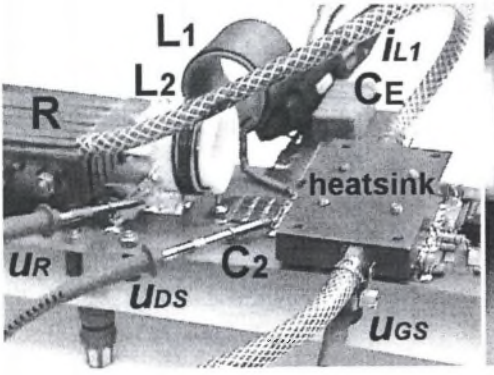

Fig. 3. Main components of laboratory inverter
Rys. 3. Zasadnicze elementy falownika laboratoryjnego

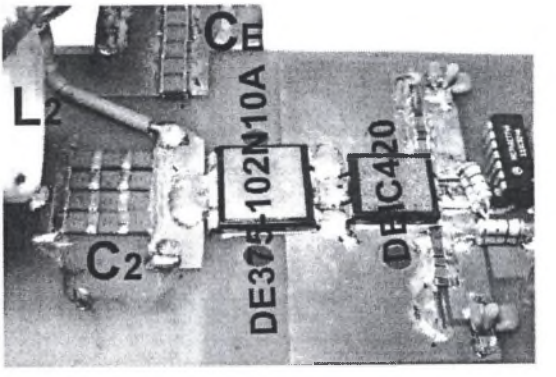

Fig. 4. DE375-102N10A MOSFET transistor and DEIC420 gate driver
Rys. 4. Tranzystor MOSFET DE375-102N10A i sterownik DEIC420

6. LABORATORY MEASUREMENTS

The laboratory inverter has been thoroughly tested. An example of the measurements is given in fig. 5. Tektronix TDS-620B 500 MHz digital oscilloscope with standard 1x10, 500 MHz voltage probes and Tektronix TCP202 current probe were used for measurements.

The selected data of inverter measurements is presented in table 1. They are: DC supply voltage E, switch "on" duty ratio D, input power P_{IN}, output power delivered to the load resistor P_{OUT}, drain efficiency η_D ($\eta_D = P_{OUT}/P_{IN} \cdot 100\%$), gate driver losses P_D and overall efficiency η ($\eta = P_{OUT}/(P_{IN} + P_D) \cdot 100\%$). In both cases switching frequency f was 16 MHz.

Table 1

Selected data of measurements

E	D	P_{IN}	P_{OUT}	η_D	P_D	η	U_{DSP}
V	-	W	W	%	W	%	V
220	0,4	907,5	799,3	88,1	23,8	85,8	750
110	0,4	209,0	189,7	90,8	22,8	81,8	343

In the first case (E=220 V) the inverter operates very close to Class E operation. The peak gate voltage is 11 V, and the peak drain voltage U_{DSP} is 750 V, safely within the manufacturer's ratings 30 V and 1000 V. The output power of the inverter is 799,3 W, drain efficiency 88,1% and overall efficiency 85,8%. The gate driver losses P_D equal the DC power consumed by the driver.

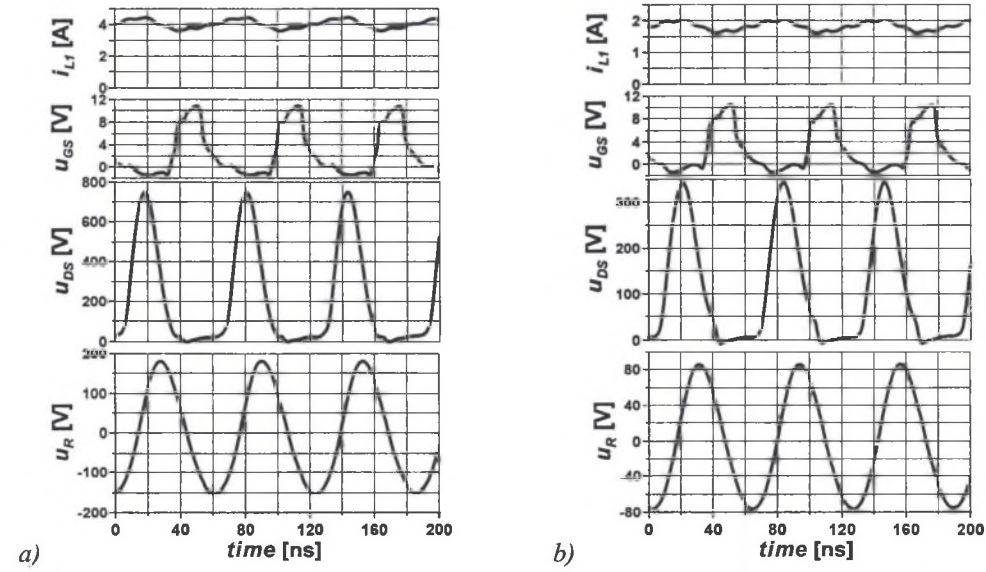

Fig. 5. Measured waveforms of currents and voltages for supply voltage E=220 V (a), and 110 V (b) (i_{L1} - supply current, u_{GS} - gate-source voltage, u_{DS} - drain-source voltage, u_R - load voltage - fig. 2)

Rys. 5. Zmierzone przebiegi prądów i napięć falownika dla napięcia zasilania E=220 V (a) oraz 110 V (b) (i_{L1} - prąd zasilania, u_{GS} - napięcie bramka-źródło, u_{DS} - napięcie dren-źródło, u_R - napięcie na obciążeniu - rys. 2)

After reducing the supply voltage E from 220 V to 110 V, the transistor is switched on at a nonzero drain-source voltage. This is caused by an increase in the effective value of the output transistor capacitance C_1, which is a nonlinear function of a drain-source voltage. Class E operation of the inverter can be achieved again by a decrease in value of the inductance L_1. It has been experimentally confirmed that the value of 3 μH is sufficient. On the other hand, precise adjustments of L_1 are not necessary for ensuring high efficiency - table 1. In general, the influence of hard-switching on inverter efficiency is insignificant when a drain-source voltage at switch-on is not higher than 50% of a DC supply voltage.

7. SPICE ANALYSIS

7.1. Class E

Analysis of the Class E inverter has been performed by means of SPICE. The DE375-102N10A MOSFET model, provided by Directed Energy, Inc. (DEI), has been used in the simulation. The SPICE model is shown in fig. 6. Its parameters of the control and the values of all components are fixed in accordance with the laboratory inverter, except the capacitor C_2, whose value has been decreased from 150 pF to 144 pF in order to ensure Class E operation.

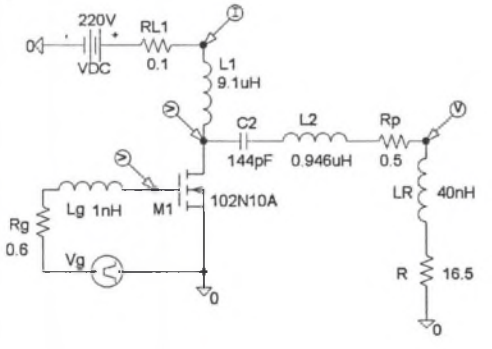

Fig. 6. Class E SPICE model, 800 W, 16 MHz
Rys. 6. Model falownika klasy E 800 W, 16 MHz w programie SPICE

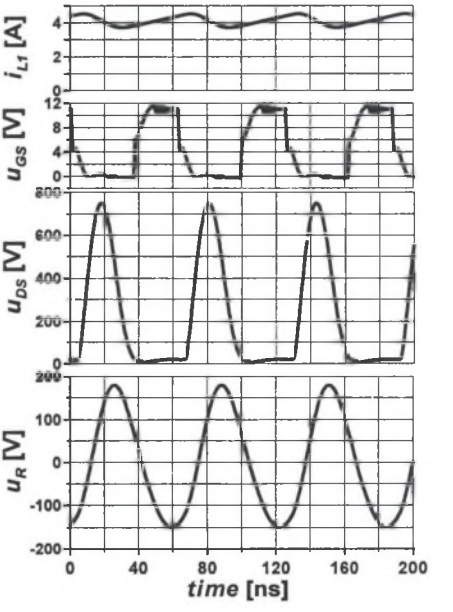

Fig. 7. Simulated waveforms of Class E SPICE model
Rys. 7. Wyniki symulacji modelu falownika klasy E w programie SPICE

There is a reasonable correlation between the SPICE model (fig. 7) and the laboratory inverter (fig. 5a). The simulation results are summarised in table 2. Among other things, the table contains power output capability c_P that is a useful factor for comparing different inverters and classes of operation. It is defined as the output power P_{OUT} that can be achieved with the peak drain-source voltage U_{DSP} of 1 V and the RMS value of the drain current I_{DRMS}

of 1 A: $c_P=P_{OUT}/(U_{DSP}\cdot I_{DRMS})$ - [4]. The value of I_{DRMS} is calculated excluding capacitive current of a MOSFET transistor. The maximum theoretical value of c_P is 0,385 for square-waveforms of drain-source voltage and drain current with the duty ratio D=0,33.

Table 2

Selected data of simulation of Class E model

E	D	P_{IN}	P_{OUT}	η_D	U_{DSP}	c_P
V	-	W	W	%	V	
220	0,4	906,8	777,4	85,7	748,9	0,16

Fig. 8 presents a graph of power output capability versus duty ratio for the Class E inverter considered in the paper. It has been calculated in MATLAB. It is clearly shown that the duty ratio D should be chosen between 0,3 and 0,4.

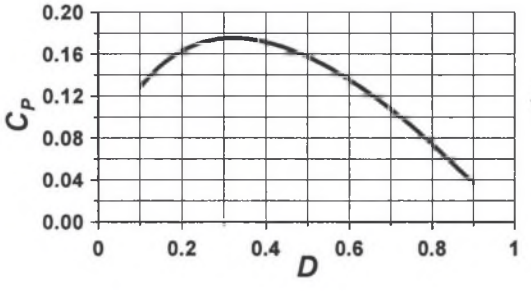

Fig. 8. Power output capability vs. switch "on" duty ratio of Class E inverter
Rys. 8. Zależność współczynnika wydajności mocowej c_P od współczynnika wypełnienia D

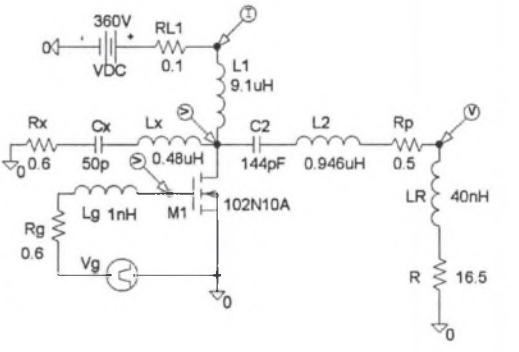

Fig. 9. Class EF SPICE model
Rys. 9. Model falownika klasy EF w programie SPICE

7.2. Class EF

In order to increase power output capability of the inverter special tuning technique has been applied. An additional series resonant circuit, tuned to the second harmonic, has been connected between the transistor drain and the ground - fig. 9. Because this technique is typical of Class F operation, where some number of harmonics is tuned to improve voltage and/or current waveforms, and at the same time Class E operation is fulfilled (fig. 10a), this idea is called Class EF operation - [6].

The simulation results of the Class EF model are shown in fig. 10. They have been achieved after proper adjustment of the inductance L_X and the duty ratio D to make the drain-source waveform u_{DS} maximally flat at the top. Further improvement is possible by employing a nonzero drain-source voltage at switch-on. This case is illustrated in fig. 10b as a result of increasing the load resistor from 16,5 Ω to 20 Ω (second row of table 3).

Several parameters for both SPICE simulations of Class EF model are grouped in table 3. The supply voltage has been changed to hold the peak drain voltage at the level of approximately 750 V. The power output capability c_P for Class EF operation (0,226) is considerably higher than the one for Class E operation (0,16).

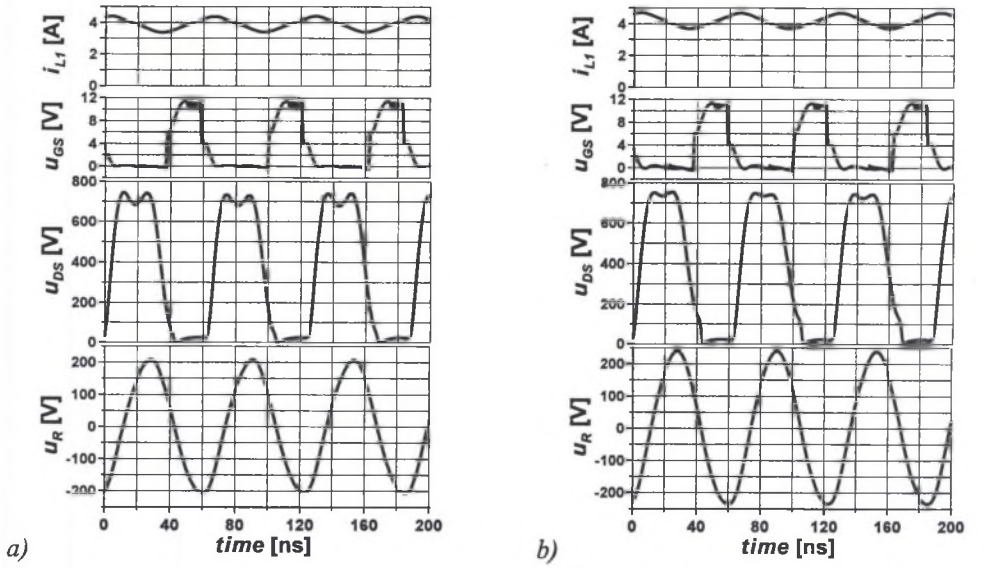

Fig. 10. Simulated waveforms of Class EF SPICE model for load resistor 16,5 Ω (a), 20 Ω (b)
Rys. 10. Wyniki symulacji falownika klasy EF dla rezystancji obciążenia 16,5 Ω (a), 20 Ω (b)

Table 3

Selected data of simulation of Class EF model

E	D	P_{IN}	P_{OUT}	η_D	U_{DSP}	c_P
V	-	W	W	%	V	
360	0,32	1414,8	1237,4	87,5	743,7	0,226
365	0,32	1527,5	1350,4	88,4	743,9	0,24

8. CONCLUSIONS

A high-efficient, 800 W, 16 MHz Class E inverter has been successfully designed, built and tested.

The inverter allows the full utilisation of the output transistor capacitance and therefore the ability to have an extremely compact design. The DE375-102N10A MOSFET transistor and the DEIC420 gate driver are the key components of the presented inverter. The inverter produces 800 W of output power with drain efficiency of 88,1% and overall efficiency of 85,8%.

The very good correlation between measurements and SPICE simulation results has been achieved. Harmonic-tuned inverters with little added circuit complexity are attractive due to their improved power output capability and/or efficiency. The solution proposed in the paper employs a series resonant circuit tuned to the second harmonic that ensures Class EF operation. Consequently, a drain-source voltage peak is reduced and power output capability increases from 0,16 (Class E operation) to 0,226 (Class EF operation). It means that inverter output power could be approximately increased by a factor of 1,4.

Further research will be focused on experimental verification of the Class EF inverter analysed in the paper.

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