STUDIA INFORMATICA

Formerly: *Zeszyty Naukowe Politechniki Śląskiej, seria INFORMATYKA*
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Volume 25, Number 4A (60)

Lech ZNAMIROWSKI

SWITCHING

VLSI Structures
Reprogrammable FPAA Structures
Nanostructures

Silesian University of Technology Press
Gliwice 2004

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CONTENTS

Spis treści

1. INTRODUCTION

This work is on switching.

Precisely, on selected problems of switching in VLSI (Very Large Scale Integration) technology, reprogrammable analog arrays technology, and nanotechnology.

Generally, a technology determines the manners of solving of classes of the definite tasks including also the manners of fabricating of products, appliances or objects.

Technologies determine the sets of constituent, basic elements (basic structures or building blocks) applied in a given technology and, next, define a set of specified operations, which have to be performed in order to obtain the desirable object or product. Technology determines operations that can be executable on active objects of this technology also, and determines the behavior of these objects. Kind and sizes of basic elements associated with different technologies are different. That it will be possible to go in this process of basic elements selection for particular technology so far, that it assumes on, that the single atoms will be these basic elements. But then, the size of the full set of operations, which have to be executed on these basic elements in order to receive the final object with desirable features, it will be excessive. In summary, and it is possible to say without care about precision, that dimensions of basic elements accepted in given technology are inversely proportional to the number of operations, which are necessary to execute on them in order to receive the desirable object. So, the choice is basic case and elaboration of such basic elements, which have decreased the number of necessary operations to execute considerably, in order to receive the required final result. Then, it is possible to say about switching between these elements accepted as basic elements, in order to structures have built about the desirable properties including also the dynamic changes of those properties. It is possible to describe the process of fabricating of these structures on the regulation of smallest elements connections, but there is not enough effective, better when the basic elements are extended more and the processes of switching determine them functions.

This is a general principle it looks to be, which meaning may be shown in case of various tasks, appliances or products, which have to be performed.

Informatics is a discipline of science dealing with the encoding, recording, processing and transferring of information or data. The works pay attention on it concerning the information processing, that it is a good practice to record the processed information in such a partial sets, which will allow on the interesting results effectively received. There will be the vectors in case of mathematical tasks, registers with multiconductor transmission lines in case of digital techniques, structure configurations in the reprogrammable electronic circuits, and conformations of molecule chains in nanostructures, but the operations are executed on these partial sets. In technical implementation, these operations come down for switching of basic elements and require a precise grasping and analysis of critical features of these processes.

Switching is exhibited in different technologies by different basic elements. The idea of this work has resulted from there, that dealing in turn with so different cases as VLSI structures, FPAA (Field Programmable Analog Array) structures and nanostructures, it is possible to notice, that the common feature takes a stand in solving the tasks related with them, rely on choice of certain basic elements critical for structure behavior as e.g. MTL (Multiconductor Transmission Lines), configurations of FPAA substructures or whole FPAA systems, molecule conformations, and it is operated on them but on the basic elements not ultra small analyzing the internal switching processes.

Consequently, by the term switching, in the work we understand the phenomenon of the state transition of structure from one stable state to another stable state, forced by external signal. The state of the structure is determined by the signal vector, the structure configuration or the structure conformation.

The proper function performed by a switched structure can be reached through the changing of the external characteristics of signals forcing changes, tuning of the structure parameters or radical change of structure configuration or conformation.

The design process of switching in a structure, usually have to fulfill the basic requirements:

the switching is possible at all,
after transition, the structure reaches a desirable state,
the speed of switching is as high as possible,
the power consumption for switching is minimized with acceptable speed of switching.

There are three main reasons of limitation in the speed of switching. Firstly, the change between stable states needs energy, enough energy (frequently in a finite time) to activate the transition. The energy can be received from external or environmental power supply or applied from switching signal source, in both cases the restricted supply's power causes the switching time extension doing it unacceptable or impossible at all. Secondly, the transient state reveals with the delay, reflections, overdamping or damped oscillations leads to elongation of the switching time. Finally, non-flexible configuration of switched structure is incapable to perform fast switching and needs external modifications.

Consequently, it is possible to say that the switching is formed by environment and internal parameters of basic elements in a structure, and the design process of switching in a structure can lead into these two directions: proper forming of the environment features in which the structure is working and selection of the internal basic elements in the switched structure for their parameters optimization.

Particularly in nanotechnology, the switching of conformations is mainly forced by environment and the post-switching state is reached when the switched nanostructure in affecting environment achieves the minimal internal, conformational energy.

In the work, in author's opinion, a critical points interrelated with the switching process in a range of mentioned above technologies are discussed, and the solutions of more important problems are presented.

1.1. Problem Formulation

In the recent VLSI design methodology, the designer of the integrated-circuit chip begins with a hierarchical description of the designed structure. Independently on the strategy of design "top-down" or "bottom-up", at the most lower level (physical level) the basis are well-designed and optimized elements forming the cell library. Cells performing elementary logic or analog operations consist passive elements and semiconductor devices connected together with a short wires forming internal interconnections. These cells connected to each other form macrocells with longer interconnections. Continuing this procedure, it is possible to produce VLSI design of enormous complexity and computing possibilities, in an ordered manner. It is worth to remember, that the interconnections between bigger macrocells (on-chip interconnections) have to be long because of dimensions of the macrocells and a distances between them.

The quality measure of the designed VLSI structure, for most integrated circuits is the speed at which they perform their operations. In the past, the speed of a chip has been largely determined by the slow semiconductor devices, placed in the cells. The influence of the capacitance of the on-chip interconnections was unimportant. Today, as the scale of integration increases and transistors become very fast and in proportion are devices of smaller power, the effect of parameters of the on-chip interconnections (capacitance, inductance, losses and reflections) plays a crucial role in the switching speed degradation. In realty, the problem of interconnections is more complex, because the data between macrocells are sent in a form of multi-bit words forming interconnections like busses, or in other words the coupled, multiconductor transmission lines. The switching features of this kind of line, depend on the internal parameters of the MTL and external (environmental) conditions in which it works.

The problems considered in the work in this area, are formulated in p. 1.1.1.

Digital circuits can be used to implement high-accuracy and high-complexity signal processing algorithms, typically for low frequency signals where power dissipation during the

operations is not critical. Analog circuits offer advantages in applications where signal frequencies are high and low power dissipation is essential. However, the accuracy of analog circuits is limited and they can not be used to implement algorithms of high complexity. As the complexity of modern processing systems grows, the traditional design with strict separation of analog and digital functions becomes impractical. Often times, it is desirable to have flexible and programmable systems such that partitioning into analog and digital circuitry can be changed during processing. Processing in a large system is assigned to analog and digital circuits to take advantage of specific circuit properties for overall performance optimization, such as power minimization. If the processing requirements and algorithms change over time, the optimal assignment of processing functions may change and dynamic reassignment of functions and reconfiguration of circuits may be necessary. A typical technology of analog circuits did not provide so far the capability of changing the circuitry once it was built up. The new technology of Field Programmable Analog Arrays (FPAA) in combination with the well known technology of Field Programmable Gate Arrays (FPGA) provides a basis for the development of a dynamically reconfigurable mixed-signal (analog/digital) hardware. For recently accessible FPAA there are two possible ways to dramatically improve the switching time of reconfiguration. One way is based on the independent switching in the internal cells of the working FPAA chip, configured by downloading process. The second way has an environmental character of changes, and needs a parallelization of working FPAA. Using two or even more of these devices in parallel it is possible to reprogram the system and reassign the circuits in real time. Switching the outputs of the FPAAs provides an uninterrupted processing of the input signal. To optimize the transitions of the switching and to speed-up the reconfiguration process it is necessary to analyze the dynamic time behavior of the reconfiguration and to model the transitions between the diverse chip in an experimental setup.

The problems considered in the work in this area, are formulated in p. 1.1.2.

If basic elements in a given technology are simple atoms or molecules, then this technology is named nanotechnology. We will focus on the mechanism of switching in organic nanostructures. More precisely, we consider the switching processes of conformation in the backbone of a chain of the amino-acid residues, forming a polypeptide synthesized in the process of translation. The mechanism of protein synthesis is a process called translation because the string of letters of the four-letter alphabet of nucleic acids accordingly with genetic code is translated into string of amino acids of the 20-amino acid alphabet, forming proteins. The process takes place in a ribosome structure in presence of at least one kind of tRNA and activating enzyme for each amino acid. The translation processes is performed in a ribosome moving along the mRNA chain, and the activated precursor is driven by ATP. Protein synthesis takes place in initiation, elongation, and termination stages. The *initiation stage* results in the connecting of the initiator tRNA to the start signal in mRNA. The *termination stage* takes place when a stop signal in the mRNA is read by the protein release factor. Each nucleotide triplet, or codon, in mRNA chain encodes a specific amino acid. In the *elongation stage*, each

molecule of tRNA binds only the amino acid proper to a particular codon, and tRNA recognize a codon by means of a complementary nucleotide sequence named anticodon. The movement of the ribosome to the next codon is powered by the hydrolysis of GTP. When the termination stage occurs, the completed polypeptide chain is released from the ribosome. Next, the switching of conformation is forced by environment's components and the post-switching state of polypeptide is reached. The conformation switching plays an important role in the processes of signal transduction pathways in the nanonetworks.

The problems considered in the work comprising this range of themes are formulated in p. 1.1.3.

1.1.1. Switching in the Interconnections of Monolithic VLSI Structures

The design of interconnects in a high-speed integrated circuits and systems requires analysis and computer simulation based on interconnects models applying the basic elements in a form of MTL [Amem67, Chan70, Rueh87, DjSH87, PLPC90, QNPS93, Sun03, Anso04]. Respective assumptions in the MTL model structure, its parameters, and environment features (drivers, receivers, substrate parameters) leads to effective simulation-based or guidelines-based process of design fulfilling the design requirements: an interconnection time delay and crosstalk [Saku93a, SaKN91, KaSa98, YaBr97], an overshoot, undershoot and rise time requirements at the receiver [YaBr96a-b, YaBr94], and the time delay reduction through the modification of interconnect configurations [NoSa01, PaZT03, Saku93b].

The fundamental parameters for description (or modeling) most often used in practice, lossless lines and lines with lossy conductors include capacitance matrices. Precisely, these are the matrices per-unit of length, the capacitance coefficients matrix called Maxwell matrix of MTL and the two-terminal capacitance matrix [Rueh87]. If the two-terminal matrix is known, the Maxwell matrix used for MTL switching characteristics estimation, can be computed from the two-terminal matrix. Computational techniques to determine the Maxwell matrix are based on geometrical data and the electrostatic field equations of multiconductor microstrip or strip lines [Rueh87, WHMS84, Week70, Kamm68]. These techniques are typically based on several approximations and the measurements are necessary for validating of computed results.

In the work (p. 2.2-2.6), two methods of determination of the Maxwell matrix from measurements are presented: passive measurements and measurements with active separation [ZnPa98b, Znam01a, PaZR01, ZnPa02, PZRG02]. The measurements were performed basing on fabricated structures ST2 and AF4 [Appendix I, PiZn93, PiZn94].

Scaling of structures is conformed to fast switching, high-speed integrated VLSI/ULSI integrated circuits design [FeAG88, Mein84]. In case when the geometrical dimensions decrease, multiconductor interconnections between parts of a system become strongly coupled MTL, which in switching moments have to be recharged with small geometry devices [Rueh79, Rueh87].

In the work (p. 2.7) the method and numerical computations of scaled (in geometrical sense) MTL for its energetical characterization – i.e. computing the energy gathered in the MTL in a quasi-static state is presented. This can be used for proper design of MTL internal, geometrical parameters in a VLSI/ULSI structures working with high-speed switching [Znam98b, SePZ01].

The results of measurements of the switching delay in the scaled in dimensions VLSI gates (p. 2.7.3), are also included [PiZn94].

Poor matching of the switched MTL reveals with reflections extending the time of switching and can be source of switching noises. The method of so called diagonal matching is presented in p. 2.8 of the work [ZnPS99].

The time of switching in the high-speed planar VLSI structures (driver and receiver gates connected via the long microstrip line) depends on dielectric properties of substrate under the signal and ground microstrip lines. Most important for fast switching is recharging of dielectric in the presence of the dielectric absorption phenomenon (dependency of the dielectric constant of solids on frequency [Cole41]).

In the work (p. 2.9), the model of dielectric absorption and its identification algorithm based on experimental data [Znam97] is presented. This model can be used for simulation of switching transients in the interconnections of different length for given technology, taking into account the dielectric absorption.

1.1.2. Switching in the Reprogrammable FPAA Structures

The facility of configuration and reconfiguration of field programmable gate arrays (FPGAs) is a source of substantial success of this approach for digital systems design. Some loss of performance and speed in comparison with an ASIC design in many applications is easily make up through their flexibility. On the other hand, it is apparent that many designs are now evolving towards mixed-signal systems. In these kind of circuits in CMOS technology, the analog part of a system and an interface are composed frequently basing on switched capacitor (SC) technology and in the newest solution basing on Field Programmable Analog Arrays [Anad01a-d, Moto97a-b, AMBA97, BrMa98, DMGu98, Vitt90, Dabr96, Mula87]. Wide area of applications of the classical (no dynamically reconfigurable) FPAAs in SC and SI (Switched-current circuits) technologies [Schm03, HuWT00] is presented in [Vitt02, BrMa98, EQOM98, PiPe98, HuBM89]. Overview of FPAA for evolvable analog spacecraft electronics contains [PSMJ03], while a future solutions of dynamically reconfigured FPAA chips and FPAA systems based on the fast switched, internally parallel FPAA cells and FPAAs/Crosspoint Switch architecture [AnDe01, AnDe02] are presented in [Znam01c].

There are two main weak points in fast switching of reconfigurable FPAA: firstly, the time of download of the configuration from supporting program or EEPROM memory with the time of transients in a FPAA chip when the download is finished and the chip undertakes

its function, and secondly, for recently accessible FPAAs, there is no possibility of switching its parameters values and a part of active structure on-the-fly (during FPAA operation).

In the work, in p. 3.2 and 3.3 the solution of fast switching of the part of working FPAA for adaptive operation is presented [ZnPV04, Znam98a, PaZn00, PaZn01]. The solution is based on external control of one or few CAB (Configurable Analog Block) in the working FPAA.

The solution of the download time problem is presented in p. 3.4 and 3.5 of the work. The solution for "hiding" of the download time and time of transients after download, in FPAA chip operating in continuous time fashion is based on parallelization of the FPAAs [ZnPR02, Znam98a, ZnPa98a]. The applications of the modified, fast switched FPAAs systems [ZnPV04, PVZH01] for adaptive and predictive control with possible application in the microreactors control are presented in p. 3.8 of the work.

1.1.3. Switching in the Nanostructures

The three-dimensional structure of a molecule can be completely described by placing it in a Cartesian coordinate system and listing *x, y, z* coordinates for each atom in the standard format [CCDE96, BWFG00]. In further investigations, we will focus on biocompatible nanostructures namely, on the methodology of modeling and simulation of the polypeptides conformation switching. When we simulate a new structure of polypeptide or switching processes of conformations of the given chain, the synthesis programs generating a spatial shape of polypeptide, use the formatted amino acids library [Klot01, Nucl01a-b] and need the information on angles between α-carbons bonded with the side chains and a contiguous peptide groups. These angles, the torsion angles, play a crucial role in the conformation of proteins because the three-dimensional structure of protein determines its biological functions or chemical activity [LBZM01, Stry94]. The changes of environment parameters and its features are the source in forcing the switching of post-translational conformation in the polypeptide chains. In the nanonetworks [Znam03a, Znam04], the molecules having a reversible conformation switching possibilities are the basic elements of signal transduction paths existing in a signal switching cascades. Recent papers treating the modeling and simulation of biocompatible nanostructures and systems [Stok00] fall into two groups. Papers of the first group take into consideration the nascent polypeptides forming [BuHL96, KFBD03], protein folding and refolding processes [Bake00, WeZY00, EMHJ00, Okam01, ElPi02], molecular switches [RMBH03, MaSc03], and paradigms of nanostructures modeling and construction [Lysh02, LacL03, RaCh03]. Papers of the second group take into consideration signaling switching in the cellular signaling systems [GSBH02, Ray99, HuMi00, JMBO01, NoZa04].

In the points 4.1 and 4.2 of the work, the simulation of the protein translation process [ZnZu02a-b, Znam01b] and the energetic approach for determination of polypeptide conformations in the switching processes are discussed. We present three methods of conformation determination in a switching processes, namely, the method based on the dynamic program-

ming algorithm [Znam02, ZnZu03, HeZZ03a], the method based on the modified Monte Carlo algorithm [WaZn04b] and the two-phase, sequential algorithm called Nascent Protein Folding [ZnZn04].

In the same points also, the post-translational modifications (switching of conformations) of the proteins present in the self-replication processes in biological nanosystems of informatics [Wegr01a-b, WeWZ02, WeWZ03a-b, WKBG03, WKZW04, WeWZ04], and nanotechnological, two-stage production processes [WeZn03, Znam04] are discussed. Basing on the hierarchical nanonetworks description introduced, the specific signal switching cascades like adenylate cyclase and phosphoinositide cascades and their fusion in nanonetworks is discussed in p. 4.3 [Znam03a, HeZZ03b]. The hierarchical description of the nanonetworks signal transduction with the conformational formula applied in this point seems to be the most effective description for the switching processes of nanostructures in the nanonetworks investigations.

Future works in range of technologies mentioned above will concern the process of synthesis understood as a choice of basic elements from a certain design space generally, and the proper switching operations those for the obtainment of the object or group of objects about required specificities including the switching operations caused by the environmental stimuli.

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2. INTERCONNECTIONS IN THE SWITCHING VLSI STRUCTURES

The interconnections between high-speed integrated circuits and systems are modeled as strongly coupled multiconductor transmission lines (MTL). Design of complete systems and analysis of switching transients in the system, requires extensive computer simulation involving model of interconnections [Amem67, Chan70, Rueh87, DjSH87, PLPC90]. To find the parameters of interconnection model, it is necessary to determine the corresponding capacitance matrix [precisely it is the Maxwell matrix of per-unit of length (PUL) capacitances]. The remaining parameters, such as inductance matrix [Week72, Rueh72, Rueh79] or line losses, are determined depending on the type of propagated waves and physical phenomena accompanying to the high-speed transmission [Chan70, WHMS84, VonH54, YeFW82, Znam97]. Considering an MTL on which the only propagation modes are TEM (transverse electromagnetic) or quasi-TEM [Marx73, KrHa70, Sche55], the distribution of voltages and currents along the lines can proceed from telegrapher's equations. A broad class of interconnections behavior is dominated by the inductive and capacitive effects, and thus these MTL may be approximated by a lossless model. In these cases, basing on capacitance and inductance matrices, the switching parameters of the equivalent MTL (e.g. the delay of each line or line impedance) to the given MTL may be found [MaEa90, TrRe85, RoSa87, PaOG89, HaTr94], as well as the MTL model suitable for use in the circuit simulators such as SPICE [Nage75].

Capacitance matrix determination is of central importance for the switching characterization of interconnections. To find the capacitance matrix it is possible to proceed in two ways. One technique to determine the capacitance matrix, is based on geometrical data, the electrostatic properties of multiconductor striplines, and computations [WHMS84, Kamm68, Rueh87, Week70, PLQP85, RuBr75]. The second approach is based on measurements, that is, calculating the capacitance matrix from the laboratory data.

In this chapter, two methods of determination of the Maxwell matrix from measurements are presented. In first approach, the capacitance matrix can be determined indirectly using the measurement of composed, "two-terminal capacitances", and calculations. This method requires very high accuracy, that is accuracy of instrument and carefully constructed measure-

ment station. Because of significant error propagation occurring in calculating the off-diagonal elements following such an approach [ZnPa98b], a second, measurement technique based on active separation of the capacitance network [ZnPa02, Znam01a, PaZR01, PZRG02, PiZn93, PiZn94] is proposed for determination of required elements of Maxwell matrix.

In design of interconnects, the scaling of transmission lines structures is conformed to fast switching of high-speed VLSI/ULSI integrated circuits [FeAG88, Mein84]. In the case when the geometrical dimensions decrease, multiconductor interconnections between parts of a system have to be recharged with small geometry devices [Rueh79, Rueh87], and proper scaling leads to the performance of structures improvement [Znam98b, SePZ01, PiZn94].

Poor matching of the switched MTL reveals with reflections extending the time of switching and can be source of switching noises. The design of matched MTL (driver's side of MTL and the far-end of MTL loaded with receivers) plays important role in the high-performance packaging [ZnPS99].

The last problem discussed in this chapter is the dependence of the switching transient time in the high-speed planar VLSI structures (driver and receiver gates connected via the long microstrip line) on the dielectric properties of substrate under the signal and ground microstrip lines. Recharging of dielectric is most important for fast switching in the presence of the dielectric absorption phenomenon [Cole41]. The simulation based on the identified model of dielectric absorption can be used for proper delay estimation, interconnections design, and technology process improvement [Znam97].

For analysis and design, the electrical data and basic dimensions we get from the silicon foundry [Grod93, Euro95b, Tomo88, Znam03b] and the geometric data from the description of the examined layout e.g. in the CIF (Caltech Intermediate Form) format [MeCo80, Znam93a-b]. For measurements, the prototypical test structures are necessary [Appendix I].

2.1. Interconnections in a VLSI Structures

General view of the coupled multiconductor transmission lines in a VLSI structure for multi-layer nonhomogeneous dielectric with n conductors and the ground-reference is presented in Fig. 2.1. The planes B_1 and B_2 denote the dielectric interfaces. Depending on the type of discussed MTL structure, one of the conductors will be selected to serve as ground conductor for the system, or can be replaced by a ground plane of infinite extent placed below and parallel to the dielectric interfaces. In the most cases we may consider one plane of dielectric interface B_1, below the conductors, with defined constant permittivity (excluding the case of dielectric absorption analysis) and constant permeability for each dielectric layer.

2.2. Passive Measurements

Consider a structure line [ZnPa98b] with n signal lines and a ground line (denoted by #0) (Fig. 2.2).

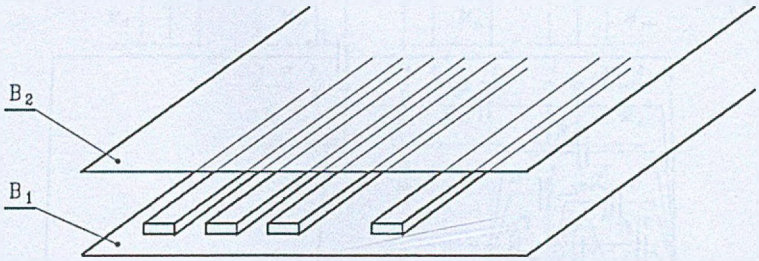


Fig. 2.1. General view of the coupled multiconductor transmission lines in a VLSI structure
Rys. 2.1. Widok ogólny sprzężonej wielolinii transmisyjnej w strukturze VLSI

For this multiconductor structure, one can use equivalent circuit presented in Fig. 2.3. "Two-terminal" capacitances giving equivalent circuit for the multilayer structure are denoted by T_{ij}. Indexes i and j designate node numbers in the structure.

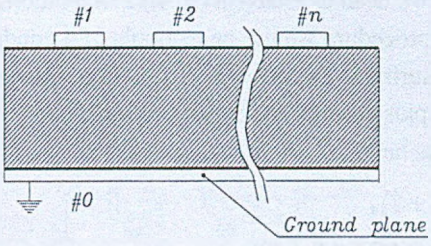


Fig. 2.2. n-Conductors geometry with reference
Rys. 2.2. Przekrój linii n przewodowej z przewodem ziemi

To simplify the notation the "two-terminal" capacitance T_{ij} from the i-th conductor to the ground is denoted by T_{ii}.

2.2.1. Measurement Procedure

During the passive (or indirect) measurements, adjacent conductors are connected together to improve upon the accuracy (inaccuracies are due to smaller parasitic capacitances that are introduced with additional conductors in contrast to the case when nonadjacent conductors are shunted using the same measurement procedure). M_{ij} denotes the measured value, that is, the capacitance of conductors i through j connected together and measured with respect to the ground.

The definition of T_{ij} and M_{ij} involves symmetry relations

$$M_{ij} = M_{ji} \tag{2.1}$$

and

$$T_{ij} = T_{ji} . \tag{2.2}$$

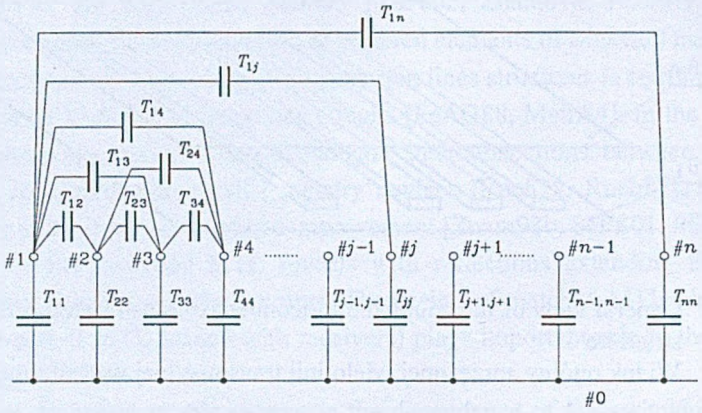


Fig. 2.3. Capacitances equivalent circuits for n conductors with reference
Rys. 2.3. Schemat zastępczy linii n przewodowej z ziemią

Thanks to the symmetry we need to establish $(n^2-n)/2+n$ relations instead of n^2 relations.

To illustrate the desired procedure we use an example of 4 conductor structure. The arrangement of conductors for measuring is shown in Fig. 2.4. The "two-terminal" capacitances of this system, composed of 4 lines plus ground, are shown in Fig. 2.5.

From Figs. 2.4 and 2.5 we have

$$\begin{aligned}
M_{11} &= T_{11} + T_{12} + T_{13} + T_{14} \\
M_{12} &= T_{11} + T_{13} + T_{14} + T_{22} + T_{23} + T_{24} \\
M_{13} &= T_{11} + T_{14} + T_{22} + T_{24} + T_{33} + T_{34} \\
M_{14} &= T_{11} + T_{22} + T_{33} + T_{44} \\
M_{22} &= T_{12} + T_{22} + T_{23} + T_{24} \\
&\cdot \\
&\cdot \\
M_{34} &= T_{13} + T_{23} + T_{33} + T_{14} + T_{24} + T_{44} \\
M_{44} &= T_{14} + T_{24} + T_{34} + T_{44}
\end{aligned} \tag{2.3}$$

In the general case for n conductors plus ground we use Fig. 2.6. Furthermore, we shall use only M_{ij} and T_{ij} for which $i \leq j$. The ground is the conductor denoted '0' in the middle of the structure. Bold lines correspond to the above example.

Because all nodes between i and j nodes are shunted, than, from Fig. 2.6 one may write:

$$M_{ij} = \sum_{k=1}^{j} \sum_{l=1}^{n} [1 - \delta_i (1 - \delta_{kl})] A_{kl} \tag{2.4}$$

for $i = 1, 2, \ldots, n$, $j = 1, 2, \ldots, n$ and $i \leq j$, and where

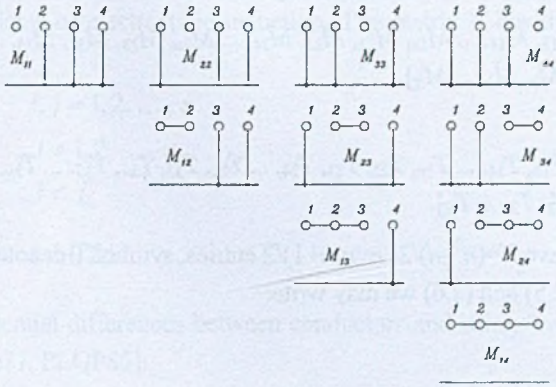


Fig. 2.4. Measurement procedure: measurements for determining measurements matrix $\boldsymbol{M} = [M_{ij}]$ where M_{ij} is the measured capacitance between non and grounded conductors (shunted to reference)

Rys. 2.4. Procedura pomiarowa: pomiary dla wyznaczenia pomiarowej macierzy $\boldsymbol{M} = [M_{ij}]$ gdzie M_{ij} jest pojemnością zmierzoną pomiędzy odpowiednimi grupami przewodów zwartych wzajemnie

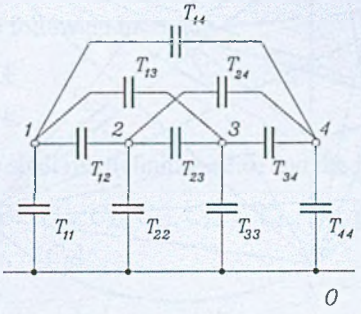


Fig. 2.5. "Two-terminal" capacitances equivalent circuit for conductors and reference

Rys. 2.5. Schemat zastępczy dla układu pojemności „dwukońcówkowych" i ziemi

$$\delta_l = \begin{cases} 1 & \text{for all } s \text{ satysfying condition } i \le l \le j \\ 0 & \text{for all remaining } l, \end{cases}$$

$$A_{kl} = \begin{cases} T_{kl} & \text{for} \quad k \le l \\ T_{lk} & \text{for} \quad k > l, \end{cases}$$

$$\delta_{kl} = \begin{cases} 1 & \text{for} \quad k = l \\ 0 & \text{for} \quad k \ne l. \end{cases}$$

Relation (2.4) describes interdependence between measured capacitances M_{ij} and "two-terminal" capacitances.

To simplify the notation we use the following vector definitions

$$M^T = [M_{11}, M_{12}, M_{13}, M_{14}, \ldots M_{1n}, M_{22}, M_{23}, M_{24}, \ldots M_{2n}, M_{33}, M_{34}, M_{35}, \ldots M_{3n}, M_{44}, \ldots M_{nn}]$$
$$= [M_1, M_2, M_3, \ldots M_N] \quad (2.5)$$

and

$$T^T = [T_{11}, T_{12}, T_{13}, T_{14}, \ldots T_{1n}, T_{22}, T_{23}, T_{24}, \ldots T_{2n}, T_{33}, T_{34}, T_{35}, \ldots T_{3n}, T_{44}, \ldots T_{nn}]$$
$$= [T_1, T_2, T_3, \ldots T_N]. \quad (2.6)$$

Vectors M and T have $N=(n^2-n)/2+n=n(n+1)/2$ entries, symbol T denotes transposition. From definitions (2.5) and (2.6) we may write:

$$M = BT \quad (2.7)$$

where matrix $\boldsymbol{B}$ is defined by (2.4).

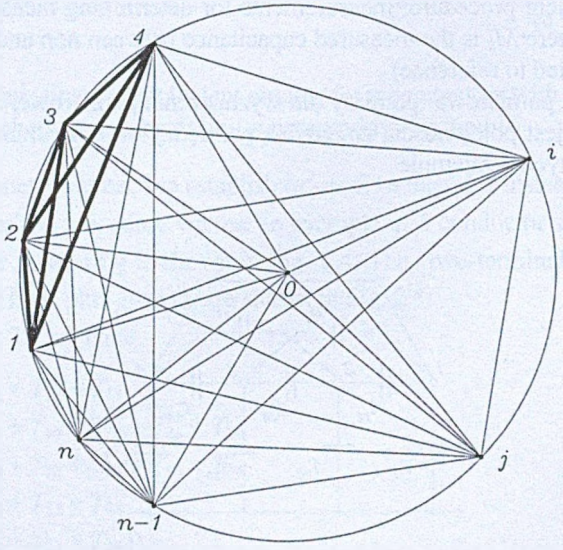


Fig. 2.6. Graph of the dependences between "two-terminal" and measured capacitances plus reference

Rys. 2.6. Graf zależności pomiędzy pojemnościami dwukońcówkowymi oraz pojemnościami zmierzonymi wraz z ziemią

2.2.2. Maxwell Matrix

Let us consider the system of n conductor plus ground (Fig. 2.3). Also, let $Q_1, Q_2, \ldots, Q_n$ be the charge per meter on the conductors with $V_1, V_2, \ldots, V_n$ the corresponding potentials. The vectors $Q = [Q_1, Q_2, \ldots, Q_n]^T$ and $V = [V_1, V_2, \ldots, V_n]^T$ are related by Maxwell matrix $\boldsymbol{C}$ ($C = [C_{ij}]$) such that [Kamm68]:

$$Q = CV. \quad (2.8)$$

The diagonal elements are called coefficients of capacitance and the off-diagonal elements are called the coefficients of electrostatic induction. The matrix C has the following properties [Kamm68, Maxw54]:

$$\begin{aligned} C_{ij} &= C_{ji} && i,j = 1,2,\ldots,n \\ C_{ii} &> 0 && i = 1,2,\ldots,n \\ C_{ij} &< 0 && i \neq j \\ \sum_{j=1}^{n} C_{ij} &> 0 && i = 1,2,\ldots,n. \end{aligned} \tag{2.9}$$

Analyzing the potential differences between conductors and using "two-terminal" capacitances T_{ij}, one finds [Pate71, PLQP85]:

$$\begin{aligned} T_{ij} &= -C_{ij} && \text{for } i \neq j \\ T_{ii} &= \sum_{j=1}^{n} C_{ij}. \end{aligned} \tag{2.10}$$

Using the symbol δ_{ij} [defined in (2.4)] and using symmetry that $T_{ij} = T_{ji}$ we obtain:

$$T_{ij} = (\delta_{ij} - 1)C_{ij} + \delta_{ij} \sum_{k=1}^{n} A_{ik} \tag{2.11}$$

for $i, j = 1, 2, \ldots, n$ and $i \leq j$.

In relation (2.11) A_{ik} has the following meaning:

$$A_{ik} = \begin{cases} C_{ik} & \text{for } i \leq k \\ C_{ki} & \text{for } i > k. \end{cases}$$

To simplify the notation we shall use definition (2.6) and the following vector:

$$\begin{aligned} C^{\mathrm{T}} &= [C_{11}, C_{12}, C_{13}, C_{14}, \ldots C_{1n}, C_{22}, C_{23}, C_{24}, \ldots C_{2n}, C_{33}, C_{34}, C_{35}, \ldots C_{3n}, C_{44}, \ldots C_{nn}] \\ &= [C_1, C_2, C_3, \ldots C_N] \end{aligned} \tag{2.12}$$

where $N = n(n+1)/2$.

Using relations (2.6) and (2.12) we may write:

$$T = DC \tag{2.13}$$

where matrix D is given by (2.11).

The relation between the measurements vector M and the vector C representing elements of Maxwell matrix can be found using (2.7) and (2.13). We have:

$$T = B^{-1}M \tag{2.14}$$

where B^{-1} is the inverse matrix of B. Finally,

$$C = D^{-1}B^{-1}M = GM \tag{2.15}$$

where D^{-1} is the inverse matrix of D and where $G = D^{-1}B^{-1}$.

Elements of the matrix C are represented by vector C in accordance with (2.12).

2.3. Error Propagation

2.3.1. General Remarks

Let

$$x=f(A, B, C, \dots) \tag{2.16}$$

be the function of arguments A, B, C, ... Let A, B, C, ... be the measurement results with absolute errors ΔA, ΔB, ΔC, ... A value of a relative error in determining x will be computed.

We can find an absolute change of x in the form [Bott75]:

$$\Delta x = \left|\frac{\partial f}{\partial A}\right|_{A_0,B_0,C_0,\dots}\cdot|\Delta A| + \left|\frac{\partial f}{\partial B}\right|_{A_0,B_0,C_0,\dots}\cdot|\Delta B| + \left|\frac{\partial f}{\partial C}\right|_{A_0,B_0,C_0,\dots}\cdot|\Delta C| + \dots \tag{2.17}$$

The absolute change Δx represents an absolute error in a calculation of x with relation to $x_0=f(A_0, B_0, C_0, \dots)$.

Applying the definition of a relative error:

$$\delta_x = \frac{\Delta x}{|x|}, \qquad \delta_A = \frac{\Delta A}{|A|}, \qquad \delta_B = \frac{\Delta B}{|B|}, \qquad \delta_C = \frac{\Delta C}{|C|}, \dots \tag{2.18}$$

the relation (2.17) can be represented in a form of relative error:

$$\delta_x = \frac{\Delta x}{|x|} = \frac{1}{|f(A,B,C,\dots)|}\left(\left|\frac{\partial f}{\partial A}\right||\Delta A|\delta_A| + \left|\frac{\partial f}{\partial B}\right||\Delta B|\delta_B| + \left|\frac{\partial f}{\partial C}\right||\Delta C|\delta_C| + \dots\right). \tag{2.19}$$

Symbols δ_A, δ_B, δ_C ... represent relative errors of measurements of the values A, B, C, ...

2.3.2. Absolute Error Propagation

From (2.15) we have:

$$C = GM \tag{2.20}$$

where

M - is the vector of measurements (dimension $N=n(n+1)/2$)

C - is the calculated vector representing elements of Maxwell matrix C

G - is the matrix ($N\times N$).

Using (2.17) we find the absolute error in C_r calculation (C_r is r-th coordinate of the vector C):

$$\Delta C_r = \sum_{s=1}^{N}|G_{rs}||\Delta M_s|, \tag{2.21}$$

where

ΔM_s - is the absolute error at measurement of the s-th element of the vector M, and r, $s = 1, 2, \dots, N$.

2.3.3. Relative Error

Using (2.18) we obtain the relative error for coordinates of vector C in the form:

$$\delta_{C_r} = \frac{\Delta C_r}{|C_r|}. \tag{2.22}$$

From (2.20) one finds:

$$C_r = \boldsymbol{G}_r M, \tag{2.23}$$

where

$\boldsymbol{G}_r$ - r-th row of the matrix $\boldsymbol{G}$.

Then, using (2.21) and (2.22) we have:

$$\delta_{C_r} = \frac{\Delta C_r}{|C_r|} = \frac{1}{|\boldsymbol{G}_r M|} \sum_{s=1}^{N} |G_{rs}| \Delta M_s|. \tag{2.24}$$

Using expression

$$\delta_{M_s} = \frac{\Delta M_s}{|M_s|}$$

for relative error of the s-th element of vector M at last we have

$$\delta_{C_r} = \frac{1}{|\boldsymbol{G}_r M|} \sum_{s=1}^{N} |G_{rs}| \delta_{M_s}| M_s|. \tag{2.25}$$

Relation (2.25) describes error propagation in C_r element calculation for given measurements of M_s elements of vector M and their relative errors of measurements.

2.3.4. Examples

Example 2.1: Properties of matrix G.

a) For two lines based on (2.15) we find:

$$\boldsymbol{G} = \begin{bmatrix} 1 & 0 & 0 \\ -0.5 & 0.5 & -0.5 \\ 0 & 0 & 1 \end{bmatrix}$$

b) For three lines we find:

$$\boldsymbol{G} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ -0.5 & 0.5 & 0 & -0.5 & 0 & 0 \\ 0 & -0.5 & 0.5 & 0.5 & -0.5 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -0.5 & 0.5 & -0.5 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

c) General case

Because the r-th row $\boldsymbol{G}_r$ of the matrix $\boldsymbol{G}$ (term $|\boldsymbol{G}_r M|$ in relation (2.25)) determines the estimate of error δ_{C_r}, Table 2.1 presents values of the sum $\left|\sum_{s=1}^{N} G_{rs}\right|$ for up to n =10 lines. Presented

values of this sum refer to the elements C_{ij} [relation (12)] of the Maxwell matrix and expression $|i-j|$ represents distance of the C_{ij} from the main diagonal.

Table 2.1

Values of the sum $\left|\sum_{s=1}^{N} G_{rs}\right|$ for main, nearest main diagonal and farther elements in matrix C

N	$\|i-j\|$		
	0	1	$\|i-j\|>1$
2	1	0.5	
3	1	0.5	0
4	1	0.5	0
5	1	0.5	0
6	1	0.5	0
7	1	0.5	0
8	1	0.5	0
9	1	0.5	0
10	1	0.5	0

From Table 2.1 we see, that errors in elements C_{ij} computation, can increase rapidly for elements beyond main ($|i-j|=0$) and measured main ($|i-j|=1$) diagonals.

Example 2.2: Error propagation for the C_{16} element of the Maxwell matrix computed for six-line structure from measurements.

For the six-line structure presented in Fig. 2.7 an assumed accuracy of measurements is 1% ($\delta_{M_s}=0.01$, $s=1, 2, \ldots, N$). We will find the Maxwell matrix from measurements and will obtain the relative error propagation (2.25) in the elements of the C matrix by calculation with a given measurements accuracy of 1%.

Measurements are realized for lines of length 6.6cm. The results of measurements written in form of measurements matrix $M=[M_{ij}, i,j=1, \ldots 6]$ are as follows:

$$\begin{bmatrix} M_{11} & M_{12} & \ldots & M_{16} \\ & & \ldots & M_{26} \\ & & & \ldots \\ & & & \ldots \\ & & & \ldots \\ & & & M_{66} \end{bmatrix} = \begin{bmatrix} 13.7 & 25.4 & 36.9 & 48.6 & 60.5 & 72.3 \\ & 13.8 & 25.7 & 37.3 & 49.1 & 60.8 \\ & & 14.0 & 25.2 & 37.8 & 49.6 \\ & & & 14.0 & 26.2 & 37.9 \\ & & & & 14.3 & 25.4 \\ & & & & & 14.3 \end{bmatrix} \quad (2.26)$$

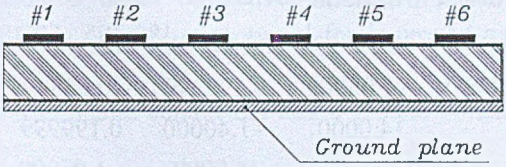


Fig. 2.7. General view of the coupled MTL in a VLSI structure
Rys. 2.7. Widok ogólny sprzężonej wielolinii transmisyjnej w strukturze VLSI

Values of capacitors are in units of pF/6.6cm. Using descriptions similar to (2.5), (2.6), (2.12) for relative error δ_{C_r} :

$$[\delta_{C_{11}}, \delta_{C_{12}}, \delta_{C_{13}}, \ldots \delta_{C_{1n}}, \delta_{C_{22}}, \delta_{C_{23}}, \ldots \delta_{C_{2n}}, \delta_{C_{33}}, \delta_{C_{34}}, \ldots \delta_{C_{nn}}] = [\delta_{C_1}, \delta_{C_2}, \delta_{C_3}, \ldots \delta_{C_N}], \quad (2.27)$$

and based on relation (2.25) and (2.27), we obtain the relative error propagation matrix for 1% measurement accuracy (Appendix II) in the following form:

$$\begin{bmatrix} 1.00000 & 25.1905 & 254.501 & 1485.02 & 1954.96 & 2426.94 \\ & 1.00000 & 25.4762 & 255.501 & 186.750 & 1973.03 \\ & & 1.00000 & 19.0000 & 258.001 & 1515.02 \\ & & & 1.00000 & 25.9524 & 172.999 \\ & & & & 1.00000 & 16.8750 \\ & & & & & 1.00000 \end{bmatrix} \quad (2.28)$$

Values of the element of the above matrix are in %.

The Maxwell matrix for measurements (2.26) has the following form:

$$\begin{bmatrix} 13.7000 & -1.05000 & -0.19999 & 0.0499992 & 0.0500011 & \underline{0.0500011} \\ & 13.8000 & -1.05000 & 0.199999 & -0.400000 & -0.0499992 \\ & & 14.0000 & -1.40000 & 0.199999 & 0.0499992 \\ & & & 14.0000 & -1.05000 & 0.300001 \\ & & & & 14.3000 & -1.60000 \\ & & & & & 14.3000 \end{bmatrix} \quad (2.29)$$

As an illustration of the error propagation in Maxwell matrix C calculations from measurement, we will present the results of changes of the element C_{16} (underlined in relation (2.29)) when sufficient elements of measurements matrix (2.26) (elements M_{15}, M_{16}, M_{25}, M_{26}) are changed accordingly with measurements error ±1%.

a) All elements of the matrix (2.26) stay unchanged except:

$M_{15} = 60.5 + 1\% = 61.105$
$M_{16} = 72.3 - 1\% = 71.577$
$M_{25} = 49.1 - 1\% = 48.609$
$M_{26} = 60.8 + 1\% = 61.408.$

We obtain Maxwell matrix in the form:

$$\begin{bmatrix} 13.7000 & -1.05000 & -0.199999 & 0.0499992 & 0.598000 & \underline{-1.16350} \\ & 13.8000 & -1.05000 & 0.199999 & -0.645498 & 0.499500 \\ & & 14.0000 & -1.40000 & 0.199999 & 0.049992 \\ & & & 14.0000 & -1.05000 & 0.300001 \\ & & & & 14.3000 & -1.60000 \\ & & & & & 14.3000 \end{bmatrix}.$$

The element C_{16} in above matrix (underlined) fell by 2426.94%.

b) All elements of the matrix (2.26) stay unchanged except:

$M_{15} = 60.5–1\% = 59.895$

$M_{16} = 72.3 + 1\% = 73.023$

$M_{25} = 49.1 + 1\% = 49.591$

$M_{26} = 60.8–1\% = 60.192.$

We obtain Maxwell matrix in the form:

$$\begin{bmatrix} 13.7000 & -1.05000 & -0.199999 & 0.0499992 & 0.497999 & \underline{1.26350} \\ & 13.8000 & -1.05000 & 0.199999 & -0.154499 & -0.599499 \\ & & 14.0000 & -1.40000 & 0.199999 & 0.0499992 \\ & & & 14.0000 & -1.05000 & 0.300001 \\ & & & & 14.3000 & -1.60000 \\ & & & & & 14.3000 \end{bmatrix}.$$

The element C_{16} in the above matrix (underlined) increased by 2426.94%.

2.3.5. Concluding Remarks

Values of the errors in C matrix computation based on indirect measurements strongly depends on G matrix and relative accuracy of measurements. As indicated by the examples, error increases when the distance of an element from the diagonal (i.e. $|i-j|$) increases. As suggested in Example 2.1, the accuracy in computation off-diagonal elements rapidly decreases. Positive value of some off-diagonal elements is caused by error propagation. This analysis indicates that the computation of matrix C from passive measurements is strongly corrupted by the measuring errors.

Using indirect measurements to finding Maxwell matrix elements requires extremely high accuracy, that is, accuracy of instrument and carefully constructed measurement station.

2.4. Measurements with Active Separation

The capacitance matrix can be determined indirectly using the measurement data and calculations (p. 2.2). Because of significant error propagation in indirect measurements

[ZnPa98b] a novel technique based on active separation of the capacitance network [Znam01a, ZnPa02, PZRG02, ZiKr88] is proposed for improved measurements of capacitance matrix.

Consider a structure with signal conductors and a ground conductor with cross-section presented in Fig. 2.8.

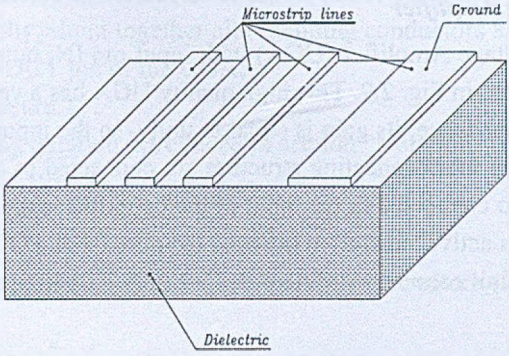


Fig. 2.8. The cross-section of n conductors geometry with reference
Rys. 2.8. Przekrój struktury wielolinii n przewodowej z ziemią

In order to determine the PUL Maxwell capacitance matrix $C=[C_{ij}]$ for this structure [Kamm68], at first we will consider the measurement technique for determination of "two-terminal" capacitance matrix $T=[T_{ij}]$ for multilayer nonhomogeneous dielectric with n conductors and the ground conductor (denoted by #0) applying active separation. The PUL Maxwell matrix is defined by Eq. (2.8), and relation between the Maxwell matrix and "two-terminal" matrix is presented by Eq. (2.10).

These "two-terminal" capacitances, T_{ij}, also called circuit capacitances have a simple interpretation presented in Fig. 2.3.

The goal of presented algorithm is determining the matrix T entries from direct measurements.

Error propagation in computing the Maxwell matrix C (the results of analysis are directly valid for "two-terminal" capacitance model i.e. the matrix T computing) of multiconductor transmission line from passive measurements was studied in [ZnPa98b]. The analysis revealed a great sensitivity of the results to measuring errors, especially for off diagonal elements of the matrix model. Consequently using such measurements to find elements of Maxwell matrices' requires instruments of extremely high, often time impractically high, accuracy. Here, a novel method for direct measurements of capacitances, T_{ij}, with the use of high-quality unity-gain operational amplifier is described. This amplifier is used to implement an active separation of conductors as described below, which allows for direct measurement of coupling capacitances. For this reason the method will be called the technique of active conductor separation or the technique for direct measurement of coupling capacitance matrix.

This measurement technique can be used in different areas of interconnections characterization [Rueh87, Znam98b] and simulation [Chan70, DjSH87, PLPC90, Znam97]. The Maxwell matrix C can be determined using the improved measurements of the T matrix.

2.4.1. Algorithm

Unity-gain Voltage Amplifier

The Unity-Gain voltage Amplifier (UGA) with input pin IN, output pin OUT and a common point G, is presented in Fig. 2.9. This high quality UGA has a very high input impedance and very low output impedance, its gain is equal to unity, so the input voltage $V_{IN}=V_{OUT}$. The conductors i and j of the interconnecting structure are connected to the pins G and IN of the UGA. This pins are also connected to the input of the capacitance meter (pins B and A in Fig. 2.10). The UGA creates active separation because the pins IN and OUT have the same potentials, and a part of a circuit connected to the pins G and OUT is charged from the output of the UGA.

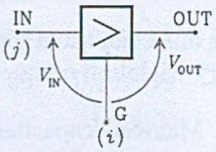


Fig. 2.9. Unity-gain voltage amplifier
Rys. 2.9. Wzmacniacz napięciowy o wzmocnieniu równym 1

Notation

For convenience of algorithm description the signal conductors are numbered from #1 to #n, and ground conductor is denoted by #0 and for the elements of matrix T_{ij} we'll use the following notation:

a) for diagonal elements when $i=j$:

$$T_{jj} \equiv T_{0j}$$

and $j=1, 2, \ldots n$.

b) for the off-diagonal elements where due to symmetry we consider that the indexes of the T_{ij} fulfill the inequality $i<j$, with $i=0, 1, \ldots n-1, j=1, 2, \ldots n$.

Measurement Algorithm

The course of measurements of the "two-terminal" capacitances, T_{ij}, can be conveniently described in the form of a measurement "algorithm" presented below.

Algorithm MATRIX-*T*-MEASUREMENT
input: n;
output: matrix T;

begin
  for i=0 to n–1 **do**
    for j=1 to n **do**
      if i<j **then**
        connect i-th conductor to the G pin of the UGA;
        connect j-th conductor to the IN pin of the UGA;
        finally, shunt together all remaining conductors and connect them to the OUT pin of the UGA;
        measure T_{ij};
        using notation introduced in section "Notation", find suitable entry of the matrix T;
end.

Let us use the graph representation of the muticonductor structure (Fig. 2.10 and 2.11).

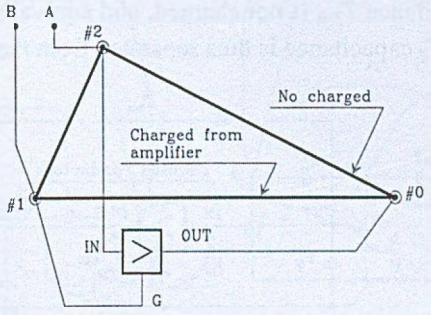


Fig. 2.10. Graph representation of measurement the capacitance T_{12} in a system of 2-conductors plus ground using the technique of active separation
Rys. 2.10. Pomiar pojemności T_{12} w systemie dwu przewodów i ziemi metodą aktywnej separacji. Reprezentacja grafowa

The nodes of the graph represent the conductors with a ground conductor and branches (bolded lines), represent the sufficient capacitances. In a 2-conductors and ground conductor system (Fig. 2.10) in a case of measuring the T_{12} capacitance, the conductor #2 connected to the IN pin of the UGA and the ground conductor #0 connected to the OUT pin of the UGA guarantees, that capacitor T_{22} has electrodes at the same potentials and is not charged. The T_{11} capacitor is charged from amplifier and in consequency, the measured capacitance T_{12} is separated from the structure. The inputs of the capacitance meter (B and A) "sees" only isolated capacitance T_{12}.

The measuring structure presented in Fig. 2.11, for exemplary 3-conductors and ground structure has similar properties.

In general, for a system of n-conductors and ground, when it is desired to measure the T_{ij} capacitance the equivalent circuit presented in Fig. 2.12 is used.

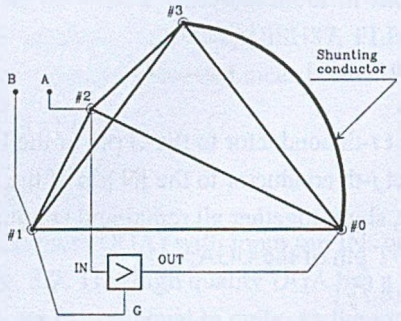


Fig. 2.11. Graph representation of measurement the capacitance T_{12} in a system of 3-conductors plus ground

Rys. 2.11. Pomiar pojemności T_{12} w systemie trzech przewodów i ziemi metodą aktywnej separacji. Reprezentacja grafowa

The equivalent capacitance T_{2eq} is not charged, and equivalent capacitance T_{1eq} is charged from the amplifier. The T_{ij} capacitance is thus separated from the circuit.

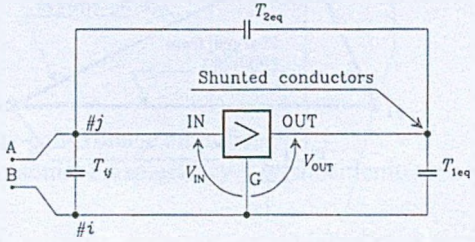


Fig. 2.12. Equivalent circuit for T_{ij} capacitance measurement with active separation in a n-conductors and ground system

Rys. 2.12. Schemat zastępczy układu pomiaru pojemności T_{ij} w systemie n przewodów i ziemi

2.4.2. Examples of Measurement Structures

Example 2.3:

To illustrate the described procedure an example of a 4-conductor interconnecting system is presented. For a 4-conductors and ground system, a complete set of connections of the active separation in the measurement circuit are presented in Figs. 2.13 and 2.14. These circuits are determined by the algorithm MATRIX-*T*-MEASUREMENT.

Example 2.4:

For a 6-conductor and ground system, the connections of the UGA fulfilling active separation during the measurements T matrix of multiconductor structure, are presented in Table 2.2.

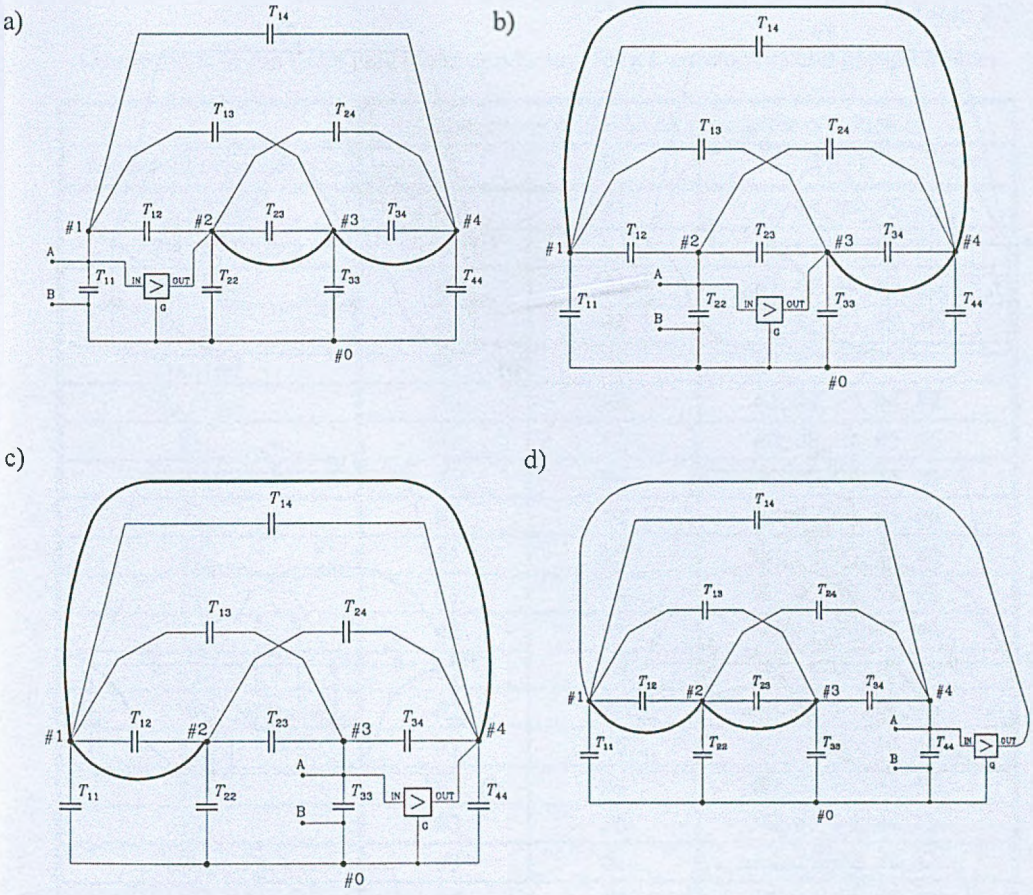


Fig. 2.13. Schematics for measurement of capacitances in a system of four-conductors and ground: a) measurement of capacitance T_{11} (T_{01}), b) T_{22} (T_{02}) measurement, c) T_{33} (T_{03}) measurement, d) T_{44} (T_{04}) measurement

Rys. 2.13. Schematy układów pomiarowych pojemności w systemie czterech przewodów i ziemi: a) pomiar pojemności T_{11} (T_{01}), b) pomiar T_{22} (T_{02}), c) pomiar T_{33} (T_{03}), d) pomiar T_{44} (T_{04})

2.5. Accuracy of the Measurements with Active Separation

2.5.1. Accuracy of the *T* Matrix Measurements

Let us assume that the relative error of a capacitance meter (compensated, full scale) is defined as δ. The measurements of the values T_{ij} entries of the matrix $\boldsymbol{T}$ when the range if instrument is properly chosen, will be bounded by the value δ, because the measurements are performed directly.

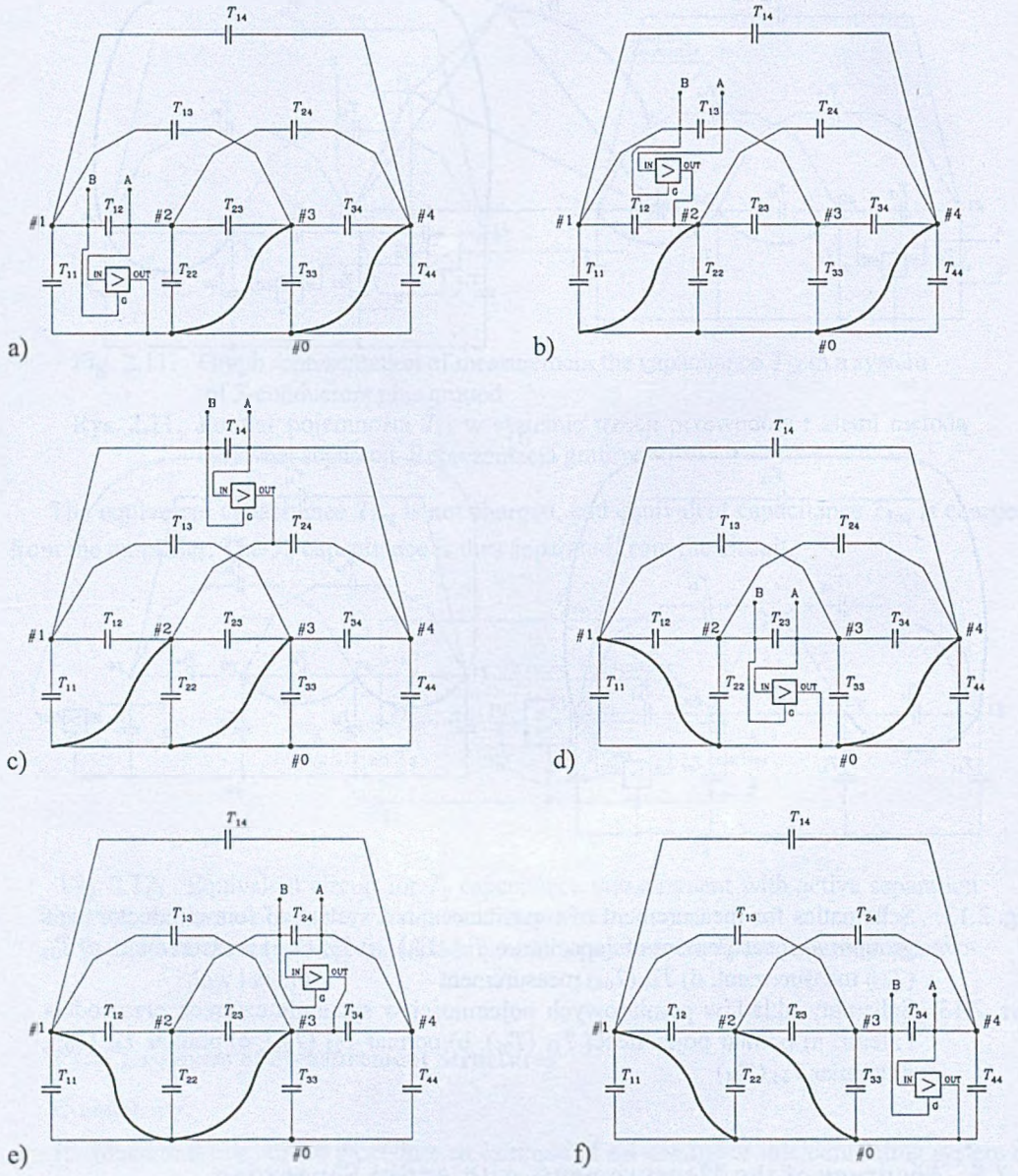


Fig. 2.14. Schematics for measurement of capacitances in a system of four-conductors and ground (continued): a) measurement of capacitance T_{12}, b) T_{13} measurement, c) T_{14} measurement, d) T_{23}, e) T_{24}, f) T_{34}

Rys. 2.14. Schematy układów pomiarowych pojemności w systemie czterech przewodów i ziemi (cd.): a) pomiar pojemności T_{12}, b) pomiar T_{13}, c) pomiar T_{14}, d) T_{23}, e) T_{24}, f) T_{34}

Table 2.2

Connections of the UGA pins to the conductors for a 6-conductors and ground system

	Connections of the UGA pins to the conductors		
Measured capacitances	G	IN	OUT
T_{11} (T_{01})	#0	#1	#2, #3, #4, #5, #6
T_{22} (T_{02})	#0	#2	#1, #3, #4, #5, #6
T_{33} (T_{03})	#0	#3	#1, #2, #4, #5, #6
T_{44} (T_{04})	#0	#4	#1, #2, #3, #5, #6
T_{55} (T_{05})	#0	#5	#1, #2, #3, #4, #6
T_{66} (T_{06})	#0	#6	#1, #2, #3, #4, #5
T_{12}	#1	#2	#0, #3, #4, #5, #6
T_{13}	#1	#3	#0, #2, #4, #5, #6
T_{14}	#1	#4	#0, #2, #3, #5, #6
T_{15}	#1	#5	#0, #2, #3, #4, #6
T_{16}	#1	#6	#0, #2, #3, #4, #5
T_{23}	#2	#3	#0, #1, #4, #5, #6
T_{24}	#2	#4	#0, #1, #3, #5, #6
T_{25}	#2	#5	#0, #1, #3, #4, #6
T_{26}	#2	#6	#0, #1, #3, #4, #5
T_{34}	#3	#4	#0, #1, #2, #5, #6
T_{35}	#3	#5	#0, #1, #2, #4, #6
T_{36}	#3	#6	#0. #1, #2, #4, #5
T_{45}	#4	#5	#0, #1, #2, #3, #6
T_{46}	#4	#6	#0, #1, #2, #3, #5
T_{56}	#5	#6	#0, #1, #2, #3, #4

2.5.2. Accuracy of the *C* Matrix Determined from the Measurement of the Matrix *T* with Active Separation

The matrix $\boldsymbol{C}$ is symmetric and because of the Eq. (2.10) the matrix $\boldsymbol{T}$ is also symmetric. Thus we can write:

$$C_{ij} = C_{ji} \tag{2.30}$$

and

$$T_{ij} = T_{ji}\,. \tag{2.31}$$

Thanks to the symmetry there are $N = \frac{n^2 - n}{2} + n$ quantities to consider instead of total n^2 matrix elements.

Using the definitions (2.6) and (2.12) we may write:

$$T=DC \tag{2.32}$$

where the dimension of matrix D is $N\times N$ and matrix D is given by (2.11).

Relation between the "two-terminal" vector T and the vector C representing elements of Maxwell matrix can be found using Eq. (2.32):

$$C=D^{-1}T=HT \tag{2.33}$$

where

$H=D^{-1}$ - inverse matrix of D.

We can find [ZnPa98b] *the absolute error* in calculation of the r-th coordinate C_r of the vector C:

$$\Delta C_r = \sum_{s=1}^{N} |H_{rs}||\Delta T_s| \tag{2.34}$$

where

$|\Delta T_s|$ - absolute error at measurement of the j-th element of the vector T,

H_{rs} - element of the matrix H, and r=1, 2, ... , N.

The relative error for coordinates of vector C has the form:

$$\delta_{C_r} = \frac{\Delta C_r}{|C_r|}. \tag{2.35}$$

From (2.33) one finds:

$$C_r = H_r T \tag{2.36}$$

where

H_r - r-th row of the matrix H.

Then using (2.34) and (2.35) we have:

$$\delta_{C_r} = \frac{\Delta C_r}{C_r} = \frac{1}{|H_r T|} \sum_{s=1}^{N} |H_{rs}||\Delta T_s|. \tag{2.37}$$

Using the definition of the relative error in capacitance measurements and the error bound we can write:

$$\delta_{T_s} = \frac{|\Delta T_s|}{T_s} \le \delta. \tag{2.38}$$

The relations (2.37) and (2.38) determine the bound for the relative error of the r-th element of the vector C in the form:

$$\delta_{C_r} = \frac{\delta}{|H_r T|} \sum_{s=1}^{N} |H_{rs}| T_s. \tag{2.39}$$

It is assumed here that the measurement accuracy of all entries T_{ij} is the same – this is the usual case with proper selection of instrument setting. Relation (2.39) gives basis for deter-

mining the relative error in calculation of element C_r from the measured values of T_s. This formula shows explicitly the effect of bound, δ, on relative errors in measurements of elements T_s on accuracy of computed elements of Maxwell matrix.

Basing on theorem demonstrated in p. 2.5.3, and simultaneously on the Remark (Eq. (2.61)), we finally get from Eq. (2.39) a very important relation:

$$\delta_{C_r} = \delta_{C_{ij}} \le \delta, \tag{2.40}$$

for all $r = 1, 2, \ldots, N$ $(i, j = 1, 2, \ldots, n,$ and $i \le j)$,

which means, that the accuracy of determining Maxwell matrix using presented method of measurements with active separation, is determined by the accuracy of measurement of the elements in "two-terminal" matrix, without any additional terms, which may be caused by error propagation in numerical calculations.

2.5.3. Mathematical Foundation of Accuracy Analysis

A. Assumptions

Let us consider the system of multiconductor planar transmission lines of n conductors plus ground conductor with cross-section presented in Fig. 2.8. Here, for convenience we will repeat some definitions and notions.

The equivalent "two-terminal" capacitance network for n signal conductors plus ground (reference) conductor is presented in Fig. 2.3. These "two-terminal" capacitances T_{ij} form a "two-terminal" matrix $\boldsymbol{T}=[T_{ij}]_{n\times n}$. The ground conductor is denoted as #0.

Let $Q_1, Q_2, \ldots, Q_n$ be the charge per unit length on the conductors with $V_1, V_2, \ldots, V_n$ the corresponding potentials. The vectors Q and V are related by Maxwell matrix $\boldsymbol{C}=[C_{ij}]_{n\times n}$ defined as follows:

$$Q = CV, \tag{2.41}$$

where:

$Q^T = [Q_1, Q_2, \ldots, Q_n]$ - is the vector of PUL charges on the n-conductor transmission line, symbol T denotes transposition,

$V^T = [V_1, V_2, \ldots, V_n]$ - is the vector of line potentials with respect to the reference.

The diagonal elements of the matrix C are called coefficients of capacitance and the off-diagonal elements are called the coefficients of electrostatic induction. The matrix C has the following properties [Kamm68]:

$$\begin{aligned} &C_{ij} = C_{ji} && i, j = 1,2,\ldots,n \\ &C_{ii} > 0 && i = 1,2,\ldots,n \\ &C_{ij} < 0 && i \ne j \\ &\sum_{j=1}^{n} C_{ij} > 0 && i = 1,2,\ldots,n. \end{aligned} \tag{2.42}$$

The goal is determination of Maxwell matrix using the results of measurements of "two-terminal" capacitances for discussed structure.

Analyzing the potential differences between conductors and using "two-terminal" capacitance matrix $T=[T_{ij}]_{n\times n}$, one finds [Rueh87]:

$$T_{ij} = -C_{ij} \quad \text{for } i \neq j,$$
$$T_{ii} = \sum_{j=1}^{n} C_{ij}. \tag{2.43}$$

These "two-terminal" capacitances, T_{ij}, also called circuit capacitances have interpretation presented in Fig. 2.3.

To simplify the notation we will use the following vector definitions (symmetry of matrix C forces the symmetry of matrix T) – thanks to the symmetry, there are $(n^2 - n)/2 + n = n(n+1)/2$ elements of matrices C and T to consider instead total n^2 elements:

$$C^{\mathrm{T}} = [C_{11}, C_{12}, C_{13}, C_{14},\ldots C_{1n}, C_{22}, C_{23}, C_{24},\ldots C_{2n}, C_{33}, C_{34}, C_{35},\ldots C_{3n}, C_{44},\ldots C_{nn}]$$
$$= [C_1, C_2, C_3,\ldots C_N] \tag{2.44}$$

and

$$T^{\mathrm{T}} = [T_{11}, T_{12}, T_{13}, T_{14},\ldots T_{1n}, T_{22}, T_{23}, T_{24},\ldots T_{2n}, T_{33}, T_{34}, T_{35},\ldots T_{3n}, T_{44},\ldots T_{nn}]$$
$$= [T_1, T_2, T_3,\ldots T_N]. \tag{2.45}$$

Vectors C and T have $N= n(n+1)/2$ entries.

Using relation (2.43) and symmetry that $T_{ij}=T_{ji}$, one may write:

$$T_{ij} = (\delta_{ij} - 1)C_{ij} + \delta_{ij}\sum_{k=1}^{n} A_{ik} \tag{2.46}$$

for $i, j = 1, 2, \ldots, n$, and $i \leq j$,

where

$$\delta_{ij} = \begin{cases} 1 & \text{for } i = j \\ 0 & \text{for } i \neq j, \end{cases}$$

$$A_{ik} = \begin{cases} C_{ik} & \text{for } i \leq k \\ C_{ki} & \text{for } i > k. \end{cases}$$

Using the definitions (2.44) and (2.45) it is possible to write (2.46) in the form:

$$T=DC \tag{2.47}$$

where the dimension of matrix D is $N\times N$.

The equation (2.47) represents the transformation mapping the N-dimensional vector C into the N-dimensional vector T, and the properties of the transformation matrix D has been precisely presented above.

B. Theorem

If the transformation matrix D (different from unity matrix – Eqs. (2.42) and (2.43)) maps the N-dimensional vector C into the N-dimensional vector T accordingly with relation

$$T = DC,$$

where vectors T, C and matrix D have properties presented in the assumptions, than the inverse matrix $H=D^{-1}$ of the matrix D is equal to itself [Znam01a] i.e.:

$$H = D^{-1} = D. \tag{2.48}$$

C. Proof

Basing on definitions of the vectors T and C, transformation (2.48) described by Eq. (2.47), can be rewritten in a form:

$$T = DC = \begin{bmatrix} D_1 \\ D_2 \\ D_3 \\ \cdot \\ \cdot \\ D_r \\ \cdot \\ \cdot \\ D_N \end{bmatrix} C \tag{2.49}$$

where

D_r - r-th row of the matrix D, and index is changing accordingly to the indexes of elements in vectors T and C ($N=n(n+1)/2$).

We also assume, that columns of the matrix D are indexed in the same manner, which allows us to write:

$$D = \begin{bmatrix} D_1 \\ D_2 \\ D_3 \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ D_r \\ \cdot \\ \cdot \\ D_N \end{bmatrix} = \begin{bmatrix} D_{11} \\ D_{12} \\ D_{13} \\ \cdot \\ D_{1n} \\ D_{22} \\ D_{23} \\ \cdot \\ D_{2n} \\ D_{33} \\ \cdot \\ D_{ij} \\ \cdot \\ D_{nn} \end{bmatrix} = [D_{rs}]_{N \times N}, \tag{2.50}$$

where $i, j = 1, 2, 3, \ldots n$, and $i \le j$; and $r, s = 1, 2, 3, \ldots N$.

The indexing of elements of matrix D is further illustrated as follows:

$$[D_{rs}]_{N\times N} = \begin{array}{c} \\ 11 \\ 12 \\ 13 \\ 14 \\ \cdot \\ 1n \\ 22 \\ 23 \\ 24 \\ \cdot \\ 2n \\ 33 \\ 34 \\ \cdot \\ 3n \\ 44 \\ \cdot \\ nn \end{array} \begin{array}{c} \begin{array}{cccccccccccccccc} 11 & 12 & 13 & 14 & \ldots & 1n & 22 & 23 & 24 & \ldots & 2n & 33 & 34 & \ldots & 3n & 44 & \ldots & nn \end{array} \\ \left[\begin{array}{cccccccccccccccc} & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \\ & & & & & & & & & & & & & & & & & \end{array}\right] \end{array} \tag{2.51}$$

Using the relations (2.46) and (2.50) one may write:

$$D_{ij} = \left[\ldots \Delta_{ij,ij} \ldots \delta_{ij,1i} \ldots \delta_{ij,2i} \ldots \delta_{ij,ii} \ldots \delta_{ij,ii+1} \ldots \delta_{ij,ii+2} \ldots \delta_{ij,in} \ldots \right] \tag{2.52}$$

where

$$\Delta_{ij,ij} = \begin{cases} -1 & \text{for } i \neq j, \text{ and is placed in } ij \text{ - th row and } ij \text{ - th column of the matrix } \mathbf{D} \text{ (Eq. (2.51))}, \\ 0 & \text{for } i = j, \text{ and is placed in } ij \text{ - th row and } ij \text{ - th column of the matrix } \mathbf{D}, \end{cases}$$

$$\delta_{ij,kl} = \begin{cases} 1 & \text{for } i = j, \text{ and is placed in } ij \text{ - th row and } kl \text{ - th column of the matrix } D, \\ 0 & \text{for } i \neq j, \text{ and is placed in } ij \text{ - th row and } kl \text{ - th column of the matrix } D, \end{cases}$$

dots ... - indicate 0's inserted in all remaining columns in considered D_{ij} row of the matrix D.

In (2.52) all numbers in the indexes ij,kl fulfill the conditions: $i \le j$ and $k \le l$. The dependence between the vectors T and C can be developed using the relations:

for $i \neq j$

$$T_{ij} = -C_{ij}, \tag{2.53}$$

for $i = j < n$

$$T_{ij} = T_{ii} = \sum_{k=1}^{n} A_{ik} = \sum_{k=1}^{i} C_{ki} + \sum_{k=i+1}^{n} C_{ik}, \tag{2.54}$$

for $i = j = n$

$$T_{ij} = T_{ii} = T_{nn} = \sum_{k=1}^{n} A_{ik} = \sum_{k=1}^{n} C_{kn}. \tag{2.55}$$

Resolving (2.54) and (2.55) for i=1, 2, 3, ... n we have:

for $i = 1$

$$T_{11} = \sum_{k=1}^{n} C_{1k},$$

for $i = 2$

$$T_{22} = \sum_{k=1}^{2} C_{k2} + \sum_{k=3}^{n} C_{2k},$$

for $i = 3$

$$T_{33} = \sum_{k=1}^{3} C_{k3} + \sum_{k=4}^{n} C_{3k}, \tag{2.56}$$

for $i = 4$

$$T_{44} = \sum_{k=1}^{4} C_{k4} + \sum_{k=5}^{n} C_{4k},$$

.

.

.

for $i = n$

$$T_{nn} = \sum_{k=1}^{n} C_{kn},$$

Let we consider the product DT of right-side multiplication of the matrix D by the vector T. Basing on the definition of vector T and Eq. (2.52) we have:

$$D_{11}T = \left[\delta_{11,11} \dots \delta_{11,12} \dots \delta_{11,13} \dots \delta_{11,14} \dots \delta_{11,15} \dots \delta_{11,1n} \dots \right] T = \sum_{k=1}^{n} T_{1k},$$

$$D_{22}T = \left[\dots \delta_{22,12} \dots \delta_{22,22} \dots \delta_{22,23} \dots \delta_{22,24} \dots \delta_{22,25} \dots \delta_{22,2n} \dots \right] T = \sum_{k=1}^{2} T_{k2} + \sum_{k=3}^{n} T_{2k},$$

$$D_{33}T = \left[\dots \delta_{33,13} \dots \delta_{33,23} \dots \delta_{33,33} \dots \delta_{33,34} \dots \delta_{33,35} \dots \delta_{33,3n} \dots \right] T = \sum_{k=1}^{3} T_{k3} + \sum_{k=4}^{n} T_{3k},$$

$$D_{44}T = \left[\ldots \delta_{44,14} \ldots \delta_{44,24} \ldots \delta_{44,34} \ldots \delta_{44,44} \ldots \delta_{44,45} \ldots \delta_{44,4n} \ldots \right] T = \sum_{k=1}^{4} T_{k4} + \sum_{k=5}^{n} T_{4k}, \quad (2.57)$$

$$\vdots$$

$$D_{nn}T = \left[\ldots \delta_{nn,1n} \ldots \delta_{nn,2n} \ldots \delta_{nn,3n} \ldots \delta_{nn,4n} \ldots \delta_{nn,5n} \ldots \delta_{nn,nn} \right] T = \sum_{k=1}^{n} T_{kn}.$$

For all remaining i,j we have (Eq. (2.53)):

$$D_{ij}T = -T_{ij}. \quad (2.58)$$

Equations (2.57) and (2.58) in a matrix notation have the form:

$$DT = \begin{bmatrix} \sum_{k=1}^{n} T_{1k} \\ -T_{12} \\ -T_{13} \\ -T_{14} \\ \vdots \\ -T_{1n} \\ \sum_{k=1}^{2} T_{k2} + \sum_{k=3}^{n} T_{2k} \\ -T_{23} \\ -T_{24} \\ \vdots \\ -T_{2n} \\ \sum_{k=1}^{3} T_{k3} + \sum_{k=4}^{n} T_{3k} \\ -T_{34} \\ \vdots \\ -T_{3n} \\ \sum_{k=1}^{4} T_{k4} + \sum_{k=5}^{n} T_{4k} \\ \vdots \\ \sum_{k=1}^{n} T_{kn} \end{bmatrix} \quad (2.59)$$

The sums of T_{ij} in Eq. (2.59) can be expressed by C_{ij} from Eqs. (2.53), (2.54), (2.55), and (2.56):

$$\sum_{k=1}^{n} T_{1k} = T_{11} + \sum_{k=2}^{n} T_{1k} = \sum_{k=1}^{1} C_{k1} + \sum_{k=2}^{n} C_{1k} + \sum_{k=2}^{n} (-C_{1k}) = C_{11},$$

$$\sum_{k=1}^{2} T_{k2} + \sum_{k=3}^{n} T_{2k} = T_{12} + T_{22} + \sum_{k=3}^{n} T_{2k} = -C_{12} + \sum_{k=1}^{2} C_{k2} + \sum_{k=3}^{n} C_{2k} + \sum_{k=3}^{n} (-C_{2k}) = C_{22},$$

$$\sum_{k=1}^{3} T_{k3} + \sum_{k=4}^{n} T_{3k} = \sum_{k=1}^{2} T_{k3} + T_{33} + \sum_{k=4}^{n} T_{3k} = \sum_{k=1}^{2} (-C_{k3}) + \sum_{k=1}^{3} C_{k3} + \sum_{k=4}^{n} C_{3k} + \sum_{k=4}^{n} (-C_{3k}) = C_{33},$$

$$\sum_{k=1}^{4} T_{k4} + \sum_{k=5}^{n} T_{4k} = \sum_{k=1}^{3} T_{k4} + T_{44} + \sum_{k=5}^{n} T_{4k} = \sum_{k=1}^{3} (-C_{k4}) + \sum_{k=1}^{4} C_{k4} + \sum_{k=5}^{n} C_{4k} + \sum_{k=5}^{n} (-C_{4k}) = C_{44},$$

$$\vdots$$

$$\sum_{k=1}^{n} T_{kn} = \sum_{k=1}^{n-1} T_{kn} + T_{nn} = \sum_{k=1}^{n-1} (-C_{kn}) + \sum_{k=1}^{n} C_{kn} = C_{nn}.$$

As a result we have:

$$DT = C. \tag{2.60}$$

The matrix D is non-singular. Indeed through the mutual subtraction of the rows and column we find, that determinant of the matrix D equals to 1 or –1, depending on the value of n. Thus we can write $T = D^{-1}C$ and considering the formula (2.47) we note that

$$D = D^{-1} = H,$$

which completes the proof.

D. Remark

From (2.52) we can observe, that row D_r (Eq. (2.50)) of the matrix D has either one column equals to –1 with all remaining columns equal 0, or few columns with all elements equal 1 with all remaining columns equal 0.

Consequently basing on the theorem we can write:

$$\frac{\sum_{s=1}^{N} |D_{rs}| T_s}{|D_r T|} = \frac{\sum_{s=1}^{N} |H_{rs}| T_s}{|H_r T|} = 1, \tag{2.61}$$

for all $r = 1, 2, 3, \ldots N$, because all elements of vector T are positive.

The symmetry of transformations of the Maxwell matrix and the "two-terminal" capacitance matrix plays a crucial role in the minimization of errors occurring in the computed Maxwell matrix from measurements performed by the direct measurement of elements of the "two-terminal" matrix using active separation of the network capacitors, The elements of Maxwell matrix are computed without any additional errors. The symmetry of transformations assures the same accuracy in computing the elements of Maxwell matrix as the accuracy of direct measurement of capacitance.

2.5.4. Examples of Measurements

Example 2.5: AF4 Structure

Example of capacitance measurement in planar lines structure composed of four-conductor metal traces (Fig. 2.16) fabricated on silicon substrate is reported in this section of the work. This test structure is called here briefly AF4 [Appendix I, PiZn94]. The purpose of this reported experiment is to illustrate the procedure for determination of Maxwell matrix of the fabricated interconnects using the measurements of "two-terminal" capacitances of the structure. The cross section of metal traces is shown in Fig. 2.18. The line designated by #0 (ground line) is the reference with respect to which the capacitance matrix is defined. The specific example system has three signal conductors and a ground/reference conductor.

The capacitance C is determined through measurement of the current flowing in the capacitor with sinusoidal voltage excitation U, under the condition $C << \frac{1}{2\pi f R_p}$, where R_p denotes the resistance in a current loop, and f is frequency of U (Fig. 2.15).

The parasities of package and external wiring capacitances (background capacitances) are eliminated by double measurement: complete IC including die with the multiconductor metal lines (MML), and package with the die removed. It is important to perform the double measurement without the external wiring changing for accurate background capacitance elimination. The idea of measurement with active isolation is presented in Fig. 2.15 and is a standard one-capacitance measurement [ZnPS99, PaZR01] with the isolation from the remaining part of the network using high quality unity-gain amplifier.

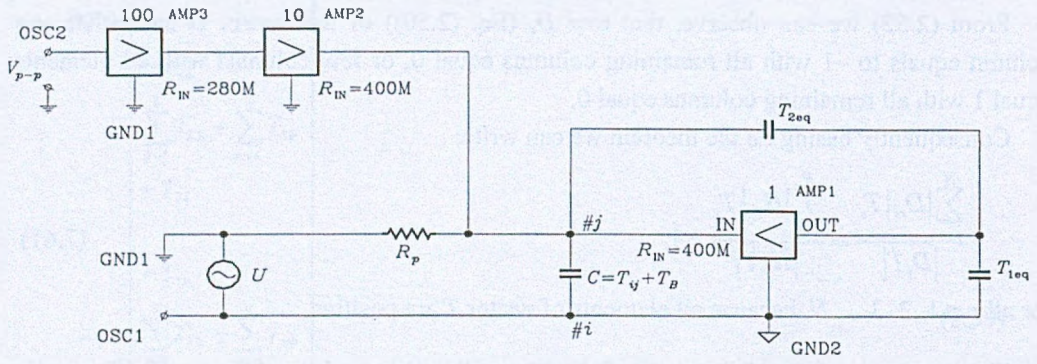


Fig. 2.15. Diagram of the measurement circuit with active separation of capacitancce in a ne work: U – sinusoidal excitation voltage 5V (peak-to-peak), T_{ij} – measured capacitanc T_B – background capacitance, R_p – resistance for current measurement equals 1.117kΩ

Rys. 2.15. Schemat układu pomiarowego z aktywną separacją pojemności w sieci: U – napięc pobudzenia 5V (peak-to-peak), T_{ij} – mierzona pojemność, T_B – pojemność tła, R_p rezystancja pomiarowa 1.117kΩ

The Unity-Gain voltage Amplifier (UGA - AMP1) with input pin IN and a common point GND2 is connected as shown in Fig. 2.15. This high quality UGA has a very high input impedance and very low output impedance, its gain is equal to unity, such that the input voltage (pin IN) is equal to the output voltage (pin OUT). The nodes *#j* and *#i* of the interconnecting structure are connected to the pins GND2 and IN of the UGA. These pins are also connected to the input of the current-measuring circuit (for $C=T_{ij}+T_B$). The UGA creates active separation because the pins IN and OUT have the same potentials (equivalent capacitance T_{2eq}), and a part of a network of capacitances (properly shunted) connected to the pins GND2 and OUT (equivalent capacitance T_{1eq}) is charged from the output of the UGA.

The phasor relations between currents and voltages in the measurement network yield

$$\frac{1000R_p}{R_p+\frac{1}{j\omega C}}=\frac{V_{p-p}}{U}e^{j\varphi}, \tag{2.62}$$

where φ is a phase shift between U and the output voltage (peak-to-peak) V_{p-p}.

After simple transformation we get:

$$C=\frac{1}{2\pi fR_p}\frac{V_{p-p}}{1000U}\frac{1}{\sqrt{1-\left(\frac{V_{p-p}}{1000U}\right)^2}}. \tag{2.63}$$

For the example network the measured capacitance is less than 20pF ($C < 20$pF), U= 5V peak-to-peak, f= 1.2kHz, and R_p= 1.117kΩ with error not greater than $0.5\cdot10^{-4}$ %, we obtain $T_{ij}=23.75\cdot10^{-12}(V_{p-p}-B)$, where T_{ij} is in [F], and $(V_{p-p}-B)$ in [V]. The symbol B represent the value obtained in the measurement of background.

Drifts of the amplifiers AMP2 and AMP3 do not introduce errors because the output voltage V_{p-p} is measured as peak-to-peak. The UGA has to be connected in different configurations in the capacitance network such that the ground system of the measurement circuit be divided into two parts: GND1 and GND2. The frequency was chosen to fulfill the condition that the amplitude of relative error is not greater than 0.002. Measurements were performed with the HP54601A oscilloscope with 8 samples average for V_{p-p} measure option.

From (2.63) we get, that the relative error of capacitance C measurement, we can estimate by a following expression:

$$\delta < \delta_R+\delta_f+2\,\delta_U. \tag{2.64}$$

where:

δ_R - relative error of resistance R_p measurement,

δ_f - frequency error,

δ_U - voltage error.

Additionally we have to take into consideration error caused by differences in geometry of package (background capacitances influence reduction) approximately equal 1%.

The measurement results of the "two-terminal" capacitance matrix for MML in a AF4 test structure, are presented in Table 2.3. In Fig. 2.16 the layout of tested interconnects (D4-L4, D3-L3, D2-L2, D1-L1) in AF4 test structure is presented.

Table 2.3

Measurement results in the AF4 test structure

Capacitance	$V_{p\text{-}p}$ [mV]	Background (B) [mV]	$V_{p\text{-}p} - B$ [mV]	Value [pF]
T_{11}	768.7	331.3	437.4	**10.39**
T_{12}	737.5	325.0	412.5	**9.80**
T_{13}	593.7	225.0	368.7	**8.76**
T_{22}	581.2	215.6	365.6	**8.68**
T_{23}	787.5	331.3	456.2	**10.83**
T_{33}	612.5	225.0	387.5	**9.20**

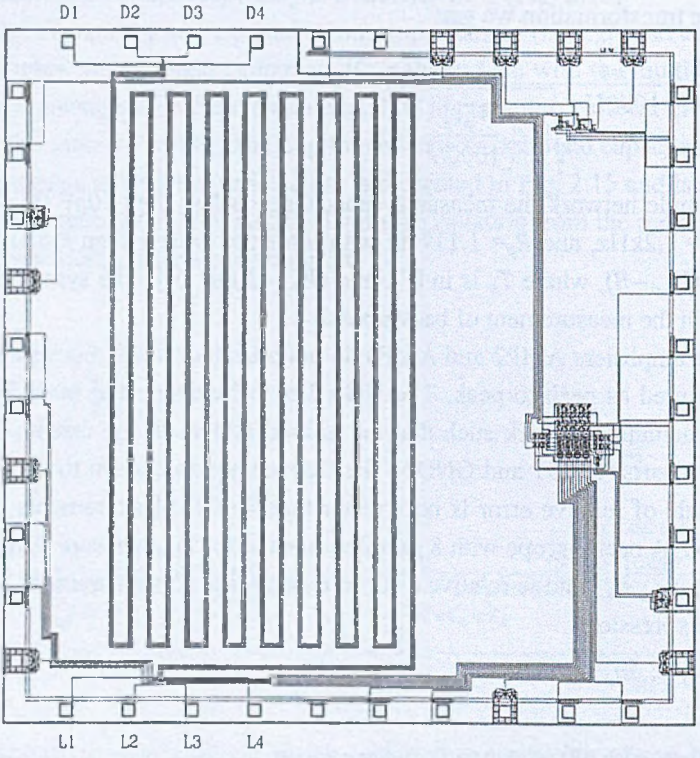


Fig. 2.16. Multiconductor metal lines (D4-L4, D3-L3, D2-L2, D1-L1) in the AF4 structure
Rys. 2.16. Wielolinie metalizacji (D4-L4, D3-L3, D2-L2, D1-L1) w strukturze AF4

Total measurement error can be estimated as 1.8% (resistance 0.5%, voltage 2·0.05%, gain reduction 0.2%, and differences in geometry of packages 1%). The measurements in-

volve pad's capacitances, capacitances of leads between pads and MML's opening, and MML all running in parallel.

The wires (metal lines) are placed approximately 1μm over the silicon/dioxide interface. On the other hand, the interface is placed over the plane y=0 on a height h equals to 1μm (Fig. 2.18). The vertical coordinate y ties clearly the coordinates of MML's vertices and dielectric interface cross-section (as a matter of fact, the differences between vertical coordinates of wires and value of h are important, but the position of y=0 is not important).

The dielectric constants are K_O=3.9 for silicon dioxide and K_S=11.8 for silicon substrate (respectively dielectric permittivity $\varepsilon_1 = K_O \cdot \varepsilon_0$ for silicon dioxide and dielectric permittivity $\varepsilon_2 = K_S \cdot \varepsilon_0$ for silicon, where $\varepsilon_0 = 8.854 \cdot 10^{-12}$ F/m – permittivity of vacuum). The thickness of metal lines is equal approximately to 1μm. The dimensions of the layout elements are presented in Fig. 2.17.

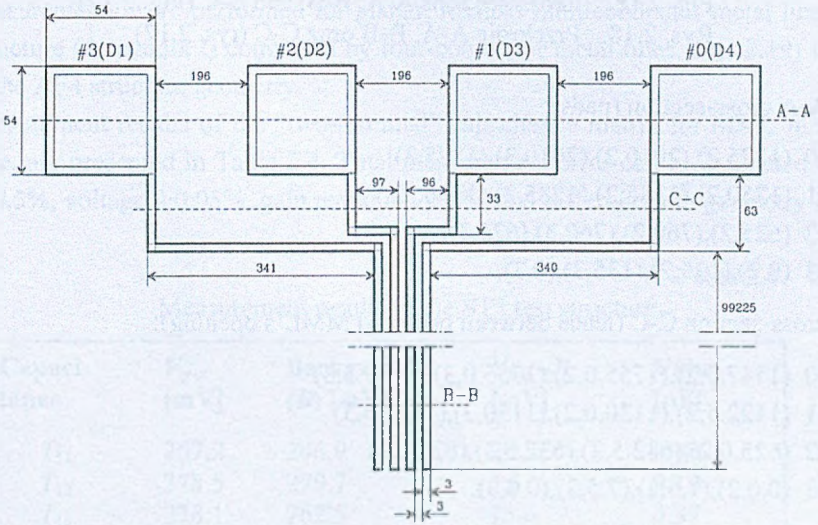


Fig. 2.17. Geometry of test interconnect in AF4 test structure. Dimensions are in design units λ=2.5μm. For clarity, the diagram is not scaled in comparing to the AF4 structure layout

Rys. 2.17. Geometria wielolinii metalizacji w strukturze testowej AF4. Wymiary przedstawiono w jednostkach projektowych λ=2.5μm. Dla większej czytelności, nie zachowano skali w stosunku do layoutu struktury AF4

The cross-section of the measured MML is presented in Fig. 2.18: A-A cross section for pads, C-C cross-section for leads between pads and MML's, and B-B for MML. Introducing all dimensions in μm, using Fig. 2.17, technological data, and the cross-section B-B of coupled lines specified as shown in Fig. 2.18, we have for B-B cross-section for MML:

#0 (45.0,2),(52.5,2),(52.5,3),(45,3)
#1 (30.0,2),(37.5,2),(37.5,3),(30.0,3)
#2 (15.0,2),(22.5,2),(22.5,3),(15.0,3)
#3 (0.0,2),(7.5,2),(7.5,3),(0.0,3).

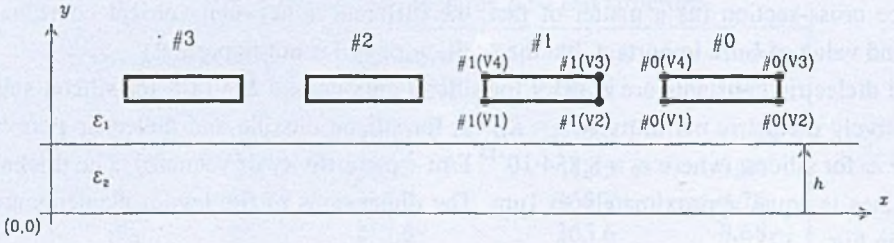


Fig. 2.18. Cross-sections A-A, B-B, and C-C (Fig. 2.17)
Rys. 2.18. Przekroje A-A, B-B oraz C-C (rys. 2.17)

For A-A cross-section (pads):

#0 (1875,2),(2010,2),(2010,3),(1875,3)
#1 (1250,2),(1385,2),(1385,3),(1250,3)
#2 (625,2),(760,2),(760,3),(625,3)
#3 (0,2),(135,2),(135,3),(0,3),

and for cross-section C-C (leads between pads and MML's opening):

#0 (1747.5,2),(1755.0,2),(1755.0,3),(1747.5,3)
#1 (1122.5,2),(1130.0,2),(1130,3),(1122.5,3)
#2 (625.0,2),(632.5,2),(632.5,3),(625.0,3)
#3 (0.0,2),(7.5,2),(7.5,3),(0.0,3).

The length of the sufficient parts of measured segment we get from Figs. 2.16 and 2.17:

length of MML:	99225μm,
length of pads:	135μm,
length of leads (approximately for two sets):	450μm.

Using geometrical and electrical data for MML in AF4 test structure (Figs. 2.17 and 2.18), we can eliminate from results (Table 2.3), the pads' capacitances and capacitances of leads between pads and MML's opening. This can be do using the computational algorithm [Week70, Kowa91] for determining the Maxwell matrix for pads and leads (cross-sections A-A and C-C in Fig. 2.17, respectively). Consequently, the values of "two-terminal" measured capacitances (Table 2.3) are decreased by 0.36% (approximately 0.28% of measured value for two sets of pads, and approximately 0.08% for two sets of leads). So, the "two-terminal" matrix for MML measurement is following in [pF]:

$$\begin{bmatrix} 10.353 & 9.765 & 8.728 \\ & 8.649 & 10.792 \\ & & 9.167 \end{bmatrix}.$$

Finally, using the accuracy analysis and programs from [Appendix II – p.6.2.2, ZnPa98b], we find the Maxwell matrix for AF4 structure from measurements in the form:

$$\begin{bmatrix} 2.907 \pm 0.052 & -0.984 \pm 0.018 & -0.880 \pm 0.016 \\ & 2.943 \pm 0.052 & -1.088 \pm 0.020 \\ & & 2.891 \pm 0.052 \end{bmatrix} \text{ [pF/cm].}$$

Example 2.6: ST2 Structure

The measurements were performed for planar, lossless multiconductor metal lines in the ST2 test structure (Appendix I) composed by four-conductor metal lines (Fig. 2.19) with different than the AF4 structure geometry.

The measurement results of the "two-terminal" capacitance matrix for MML in the ST2 test structure, are presented in Table 2.4. Total measurement error can be estimated as 1.8% (resistance 0.5%, voltage 2·0.05%, gain reduction 0.2%, and differences in geometry of packages 1%).

Table 2.4

Measurement results in the ST2 test structure

Capacitance	$V_{p\text{-}p}$ [mV]	Background (B) [mV]	$V_{p\text{-}p} - B$ [mV]	Value [pF]
T_{11}	267.2	246.9	20.3	**0.48**
T_{12}	378.5	279.7	7.8	**0.19**
T_{13}	278.1	262.5	15.6	**0.37**
T_{22}	228.1	207.8	20.3	**0.48**
T_{23}	364.1	348.9	15.2	**0.36**
T_{33}	245.3	212.5	32.8	**0.78**

The dielectric constants are K_O=3.9 for silicon dioxide and K_S=11.8 for silicon substrate (respectively dielectric permittivity $\varepsilon_1 = K_O \cdot \varepsilon_0$ for silicon dioxide and dielectric permittivity $\varepsilon_2 = K_S \cdot \varepsilon_0$ for silicon, where $\varepsilon_0 = 8.854 \cdot 10^{-12}$ F/m – permittivity of vacuum). The thickness of metal lines is equal approximately to 1μm. The dimensions of the layout elements are presented in Fig. 2.20.

In reality the measurements involve pad's capacitances, capacitances of leads between pads and MML's opening, and MML all running in parallel. In Fig. 2.19 the layout of tested interconnects (L4, L3, L2, L1) in ST2 test structure is presented. The wires (metal lines) are placed approximately 1μm over the silicon/dioxide interface. The cross-section of the measu-

red MML is presented in Fig. 2.21: A-A cross section for pads, C-C cross-section for leads between pads and MML's, and B-B for MML.

Introducing all dimensions in μm, using Fig. 2.20, and technological data, the cross-section B-B of coupled lines is specified as shown in Fig. 2.21.

Then we have for B-B cross-section for MML:

#0 (60,2),(70,2),(70,3),(60,3)
#1 (40,2),(50,2),(50,3),(40,3)
#2 (20,2),(30,2),(30,3),(20,3)
#3 (0,2),(10,2),(10,3),(0,3).

For A-A cross-section (pads):

#0 (750,2),(885,2),885,3),(750,3)
#1 (500,2),(635,2),(635,3),(500,3)
#2 (250,2),(385,2),(385,3),(250,3)
#3 (0,2),(135,2),(135,3),(0,3),

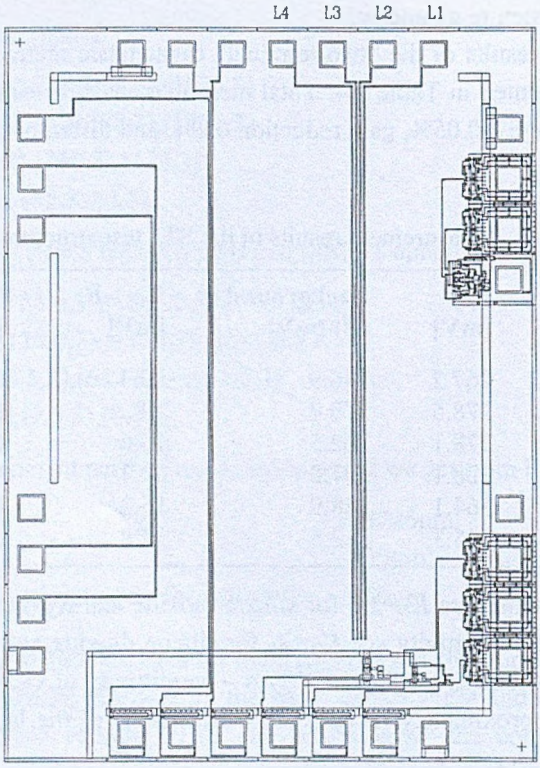


Fig. 2.19. Multiconductor metal lines in the ST2 structure
Rys. 2.19. Wielolinie transmisyjne metalizacji w strukturze ST2

and for cross-section C-C (leads between pads and MML's opening):

#0 (500,2),(510,2),(510,3),500,3)
#1 (375,2),(385,2),(385,3),(375,3)
#2 (250,2),(260,2),(260,3),(250,3)
#3 (0,2),(10,2),(10,3),(0,3).

Length of the parts of the measured segment from Fig. 2.20 are: MML 2730μm, pads 135μm, and leads 85μm.

Using geometrical and electrical data for MML in the ST2 test structure (Figs. 2.20 and 2.21), we eliminate from results (Table 2.4), the pads' capacitances and capacitances of leads between pads and MML's opening. This can be do using the computational algorithm [Week70, Kowa91] for determining the Maxwell matrix for pads and leads (cross-sections A-A and C-C in Fig. 2.20, respectively).

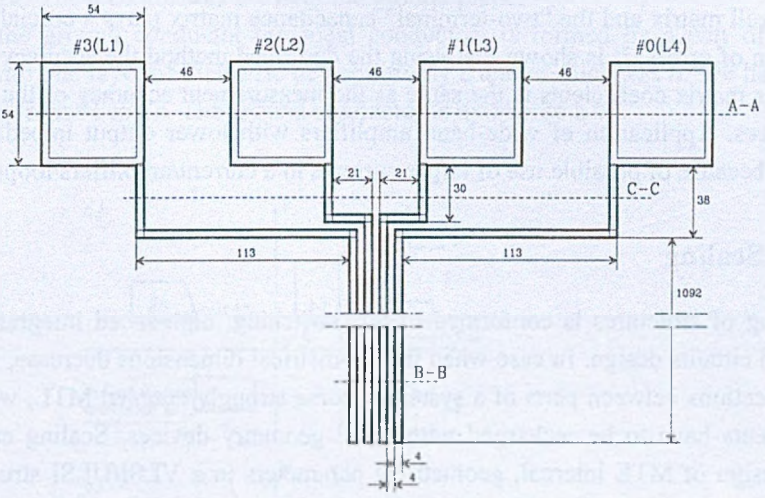


Fig. 2.20. Geometry of test interconnect in ST2 test structure. Dimensions are in design units λ=2.5μm

Rys. 2.20. Wielolinie połączeń w strukturze testowej ST2. Wymiary podane w jednostkach projektowych λ=2.5μm

Consequently, the values of "two-terminal" measured capacitances (Table 2.4) are decreased by 6.66% (approximately 4.9% of measured value for pads, and 1.76% for leads). So, the "two-terminal" matrix for MML measurement is following (in [pF]):

$$\begin{bmatrix} 0.448 & 0.177 & 0.345 \\ & 0.448 & 0.336 \\ & & 0.728 \end{bmatrix}.$$

Finally, using the error analysis and programs analogous to that presented in Example 2.5, the Maxwell matrix for the ST2 structure determined on the basis of measurements is represented in the form:

$$\begin{bmatrix} 3.553 \pm 0.064 & -0.648 \pm 0.012 & -1.264 \pm 0.023 \\ & 3.520 \pm 0.063 & -1.231 \pm 0.022 \\ & & 5.161 \pm 0.093 \end{bmatrix} \text{ [pF/cm].}$$

2.5.5. Concluding Remarks

The algorithm for improved measurements of the "two-terminal" matrix (per-unit-length) of multiconductor transmission lines for VLSI interconnections model and a methodology for calculating the elements of Maxwell matrix has been presented. The measuring technique is based on active separation of the capacitance network implemented using a high quality unity-gain voltage amplifier. The active separation significantly increases the accuracy of determining the Maxwell matrix in comparison with the indirect method. The symmetry of transformations of the Maxwell matrix and the "two-terminal" capacitance matrix plays a crucial role in the minimization of errors. It is shown that using the described method the accuracy of determining Maxwell's matrix coefficients is the same as the measurement accuracy of the "two-terminal" capacitances. Application of wide-band amplifiers with lower output impedances increases accuracy because of possible use of larger currents in a current/amplifiers loops.

2.6. Scaling

Scaling of structures is conformed to fast switching, high-speed integrated VLSI/ULSI integrated circuits design. In case when the geometrical dimensions decrease, multiconductor interconnections between parts of a system become strongly coupled MTL, which in switching moments have to be recharged with small geometry devices. Scaling can be used for proper design of MTL internal, geometrical parameters in a VLSI/ULSI structures working with high-speed switching. In this point, the results of measurements of the switching delay in the scaled in dimensions VLSI gates, are also included.

2.6.1. Energetical Characterization of MTL

Models of the MTL and simulation tools using those models [Amem67, Chan70, DjSH87, PLPC90] are usually determined for particular simulation task in connection with special boundary conditions and geometrical data extracted from layout [Kamm68, Rueh79, Week70]. For our goal, i.e. quasi-static energetical characterization of MTL representing interconnections in VLSI/ULSI structures when the scaling (width and high of planar conductors, and distance between them) takes place, we will use a model based on a layout description and cross-sectional characterization described in [Chan70, Week70]. We will build the model basing on a capacitance/inductance cross-sectional slice parameters as a per-unit-length (PUL) capacitance and a PUL inductance for nonhomogeneous dielectric medium, with the conductors resistance (PUL) network in a serial connection. It is possible to extend the model introducing nonhomogenuity, nonisotrophy, skin-effect, dielectric dispersion and absorption

effects using direct physical models for those phenomena [Znam97, HaFY71, YeFW82]. We will consider a geometrical configuration for cross-sections of MTL, shown in Fig. 2.21 (a through c).

In all cases the conductors are ideal (a capacitance network). The conductors' resistances excluding ground, are assumed to be connected in serial in z direction (perpendicular to the x-y plane) with conductors' capacitances and inductances network.

In case a) (Fig. 2.21), the space is divided into two halfspaces; the first with dielectric permittivity ε_1, and the second with ε_2. The plane of the dielectric interface is for $y=h$ with infinite dimension. The finite dimensional ideal ground conductor has potential equal to zero.

In case b), the dielectric interface plane and ground plane are of infinite extent and they are parallel to each other. The dielectric interface is at height h above the ground plane being an ideal conductor. The n conductors are over the ground plane.

In case c), the ground conductor (an ideal conductor) is formed by a pair of parallel ground planes with one layer of dielectric of permittivity ε and of thickness h. We have numbered conductors from #1 to #n. The ground conductor is numbered a #0.

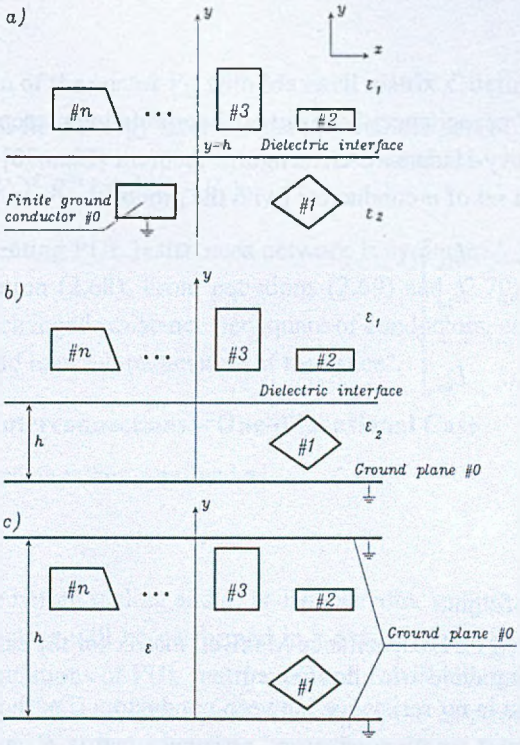


Fig. 2.21. Cross-section for the MTL cases
Rys. 2.21. Przekroje wielolinii MTL

In order to determine the PUL capacitance coefficients matrix i.e. the Maxwell matrix C for multilayer nonhomogeneous dielectric and n conductors (and the ground) imbedded, we have a basic equation for the matrix $C=[C_{ij}]$ definition:

$$\begin{bmatrix} Q_{1,1} \\ Q_{1,2} \\ \cdots\cdots \\ Q_{1,n} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & \cdots\cdots & C_{1n} \\ C_{21} & C_{22} & \cdots\cdots & C_{2n} \\ \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots \\ C_{n1} & C_{n2} & \cdots\cdots & C_{nn} \end{bmatrix} \cdot \begin{bmatrix} V_{1,1} \\ V_{1,2} \\ \cdots\cdots \\ V_{1,n} \end{bmatrix}, \tag{2.65}$$

where:

$Q_1^T = [Q_{1,1}, Q_{1,2}, \ldots, Q_{1,n}]$ – is a PUL charges vector of a n-conductor MTL,

$V_1^T = [V_{1,1}, V_{1,2}, \ldots, V_{1,n}]$ – is a corresponding voltages vector.

Properties of the matrix C are discussed in [Kamm68, Week70]. We will use the approach [Kamm68] generalized in [Week70] to find C_{ij}. Using the calculated PUL capacitance coefficients C_{ij}, we can do its object illustration using the "two-terminal" capacitance matrix T can be found [Pate71], with following elements:

$$\begin{aligned} T_{ij} &= -C_{ij} \quad \text{for } i \neq j, \\ T_{ij} &= \sum_{j=1}^{n} C_{ij}. \end{aligned} \tag{2.66}$$

These "two-terminal" capacitances have simple interpretation presented in Fig. 2.22.

We can apply the Levy-Hadamard-Gerschgorin theorem [Chan70] to calculate the PUL inductance matrix L for a set of n-conductors (with the ground):

$$L = \begin{bmatrix} L_{11} & L_{12} & \cdots\cdots & L_{1n} \\ L_{21} & L_{22} & \cdots\cdots & L_{2n} \\ \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots \\ L_{n1} & L_{n2} & \cdots\cdots & L_{nn} \end{bmatrix} \tag{2.67}$$

from equation:

$$L = \frac{1}{v_0^2} C_0^{-1}, \tag{2.68}$$

where:

v_0 – velocity of light,

C_0^{-1} – the inverted PUL capacitance Maxwell matrix for the same structure with surrounding dielectric all removed.

We assume, that there is no resistance between conductors (i.e. there are no leakage currents), therefore the per-unit-length conductors' resistance matrix R can be simply calculated from the resistance per square, and width of the conductors.

In order to discuss the energy properties of the "slice" of MTL with cross-section described above, we assume that the three-part "slice" is a serial "circuit" with PUL capacitan-

ces, PUL inductances and PUL resistances of the conductors connected serially in z axis direction (perpendicular to the x-y plane). We assume also, that the thickness of the "slice" is l (in z axis direction).

Using the diagram presented in Fig. 2.22 for orientation, let we discuss the energy gathered in the "slice", in a quasi-static state (the voltage vectors V_1 and V_2 "holding up" the "slice" are constant) but in dependency on geometrical dimensions of the cross-section of the MTL.

The first side of the MTL "slice" is connected to the voltage vector V_1, which coordinates are numbered as conductors, and reference is shunted to the ground plane (Fig. 2.21). We will consider the case with the ground as an ideal conductor. The second side of MTL "slice" is connected to the vector V_2 in the same manner. We have the capacitance network connected to the vector V_1, the resistance network supplied by V_1–V_2 voltage vector and the inductance network supplied with the current vector $l^{-1}R^{-1}(V_1–V_2)$, where R is the per-unit-length resistance matrix for the conductors and l is the thickness of the "slice".

The electrostatic energy of the capacitance part of the "slice" can be expressed as follows:

$$E_C = \frac{l}{2} V_1^T C V_1, \tag{2.69}$$

where:

V_1^T – transposition of the vector V_1, with Maxwell matrix C defined by (2.65).

The static magnetic field energy stored in the inductances part of the "slice" is:

$$E_L = \frac{1}{2l}(V_1 - V_2)^T R^{-1} L R^{-1}(V_1 - V_2), \tag{2.70}$$

since matrix R representing PUL resistances network is symmetric. Inductance matrix L was determined from equation (2.68). From equations (2.69) and (2.70) result, that for constant vectors V_1, V_2, and unchanged resistance per square of conductors, energies E_C and E_L depend only on geometrical and material parameters of the "slice".

2.6.2. Scaling of Interconnections – One-dimensional Case

Let us introduce a scale factor α defined as:

$$d' = \frac{d}{\alpha}, \tag{2.71}$$

where d is the distance before scaling and d' is distance after scaling.

Scaling of the structure will be performed in x axis (Fig. 2.21). The geometrical dimensions in x axis for calculations of PUL matrices C and L will change with a scale factor α. In case when the voltage vectors V_1 and V_2 are unchanged, the electrostatic energy will depend on the value of α. For large value of α, the charge will merely gather between the conductors working as a small multilayer capacitor; for small values of α, the charge will merely gather between the conductors and the ground plane conductor (Fig. 2.22). As a consequence, we

can look for such a value of α, when the electrostatic energy is at minimum. In parallel, we can observe changes in the level of a static magnetic field energy stored in the structure. We will apply an optimization procedure for matrix C in order to determine such a value of α, when the value of E_C is at minimum. Formally, the procedure can be expressed by:

$$E_C = \min_{\alpha \in [\alpha_{min}, \alpha_{max}]} \left\{ \frac{l}{2} V_1^T C V_1 \right\}, \tag{2.72}$$

in the range $[\alpha_{min}, \alpha_{max}]$.

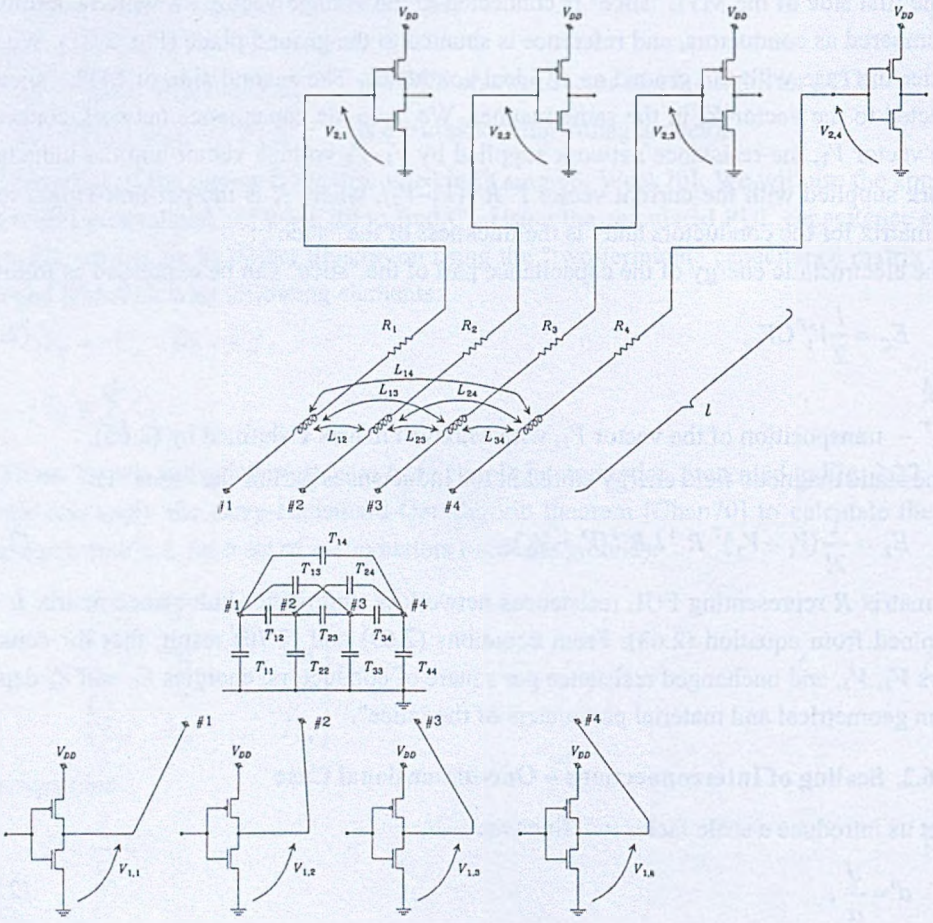


Fig. 2.22. Part of CMOS circuit, including the driving inverters, the "slice" MTL line, and the load inverters

Rys. 2.22. Wielolinia CMOS zawierająca inwertery sterujące, "plasterek linii" MTL oraz inwertery obciążenia

Example 2.7:

We will present the results of C, L and R matrices calculations and energetical characterization for a scaled, multiconductor transmission line on a cross-section *A–A* (Fig. 2.23) in a

certain chip structure. The length of 4 conductors in perpendicular direction (z-axis direction) to cross-section is l=1cm, and resistance per square is R_s=0.05Ω/□. The cross-section view of the MTL is presented in Fig. 2.24 (case b in Fig. 2.21), with conductors embedded in SiO_2 dielectric over a silicon substrate (for silicon oxide $\varepsilon_1 = K_O\varepsilon_O$ with dielectric constant $K_O = 3.9$, for silicon $\varepsilon_2 = K_S\varepsilon_O$ with dielectric constant $K_S = 11.8$ and permittivity of vacuum ε_O=8.854·10^{-12} F/m).

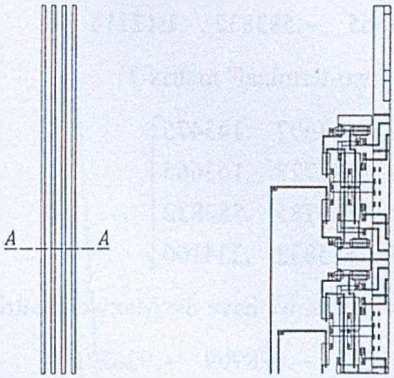


Fig. 2.23. The top view of an *A–A* cross-section for four conductors on a part of the structure
Rys. 2.23. Widok z góry przekroju *A-A* dla czterech przewodów na fragmencie struktury

The structure is supplied with two voltage vectors V_1 and V_2 in the following forms:

V_1^T=[5, 4.5, 4, 3.5] [V], and V_2^T=[2.5, 2, 1.5, 1] [V].

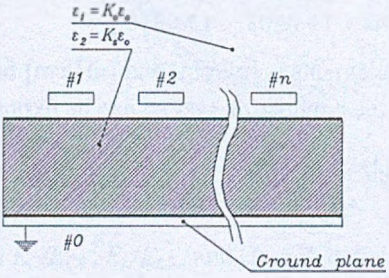


Fig. 2.24. The cross-section of the MTL (n=4; cross-section *A–A* in Fig. 2.23)
Rys. 2.24. Przekrój *A-A* wielolinii (n=4; przekrój *A-A* z rys. 2.23)

The geometrical data are following: the distance between the ground plane and a dielectric interface is h=501μm, the coordinates in [μm] of the rectangular conductor's vertices counter-

clockwise for a conductor #1 are (1,502/3,502/3,503/1,503), for a conductor #2 (5,502/7,502/7,503/5,503), for #3 (9,502/11,502/11,503/9,503); and for #4 (13,502/15, 502/15,503/13,503).

Using the program MM [Kowa91] for case b (Fig. 2.21) we get the Maxwell matrix C:

$$C = \begin{bmatrix} 1.12736 & -.584106 & -.163607 & -.145475 \\ -.584106 & 1.42034 & -.522727 & -.163665 \\ -.163607 & -.522727 & 1.41995 & -.583832 \\ -.145475 & -.163665 & -.583832 & 1.12713 \end{bmatrix}$$

From Eq. (2.66) we get the "two-terminal" matrix T:

$$T = \begin{bmatrix} .234176 & .584106 & .163607 & .145475 \\ .584106 & .149844 & .522727 & .163665 \\ .163607 & .522727 & .149785 & .583832 \\ .145475 & .163665 & .583832 & .234160 \end{bmatrix}$$

Repeating calculations for vacuum, we have the Maxwell matrix C_0:

$$C_0 = \begin{bmatrix} 0.231638 & -.143737 & -.028909 & -.026229 \\ -.143737 & 0.319769 & -.129688 & -.028919 \\ -.028909 & -.129688 & 0.319803 & -.143783 \\ -.026229 & -.028919 & -.143783 & 0.231704 \end{bmatrix}$$

Finally, basing on Eq. (2.68), we find the inductance matrix L in the form:

$$L = \begin{bmatrix} 13.8830 & 11.0209 & 9.77694 & 9.01412 \\ 11.0209 & 13.7690 & 10.9756 & 9.77696 \\ 9.77694 & 10.9756 & 13.7688 & 11.0208 \\ 9.01412 & 9.77696 & 11.0208 & 13.8816 \end{bmatrix}.$$

The unit of the C, C_0 and T elements is [pF/cm] and [nH/cm] for elements of the matrix L.

The resistance matrix R for the conductors system can be expressed as a diagonal matrix:

$$R = diag\,[R_1, R_2, R_3, R_4], \tag{2.73}$$

with elements:

$$R_i = \frac{\left(R_S \cdot \frac{l}{w}\right)}{l} = R_S \cdot \frac{1}{w}, \tag{2.74}$$

(w is the width of conductors), therefore, for the given data we have:

$$R = diag\,[250, 250, 250, 250].$$

The unit of the R elements is [Ω/cm].

From Eqs. (2.69) and (2.70) for given vectors V_1 and V_2 we can find (SCALING program – Appendix II) the values of electrostatic and static magnetic field energies stored in the structure:

$$E_{C0} = 7.61551\text{pJ}, \quad \text{and} \quad E_{L0} = 8.92365\text{pJ}.$$

For the same structure, we will find relations between energies E_C, E_L, and a scaling factor α. The scaling takes place in x direction with $\alpha = \alpha_x$. Scale for y and z directions is unchanged ($\alpha_y = \alpha_z = 1$). Results of computations are presented in Fig. 2.25.

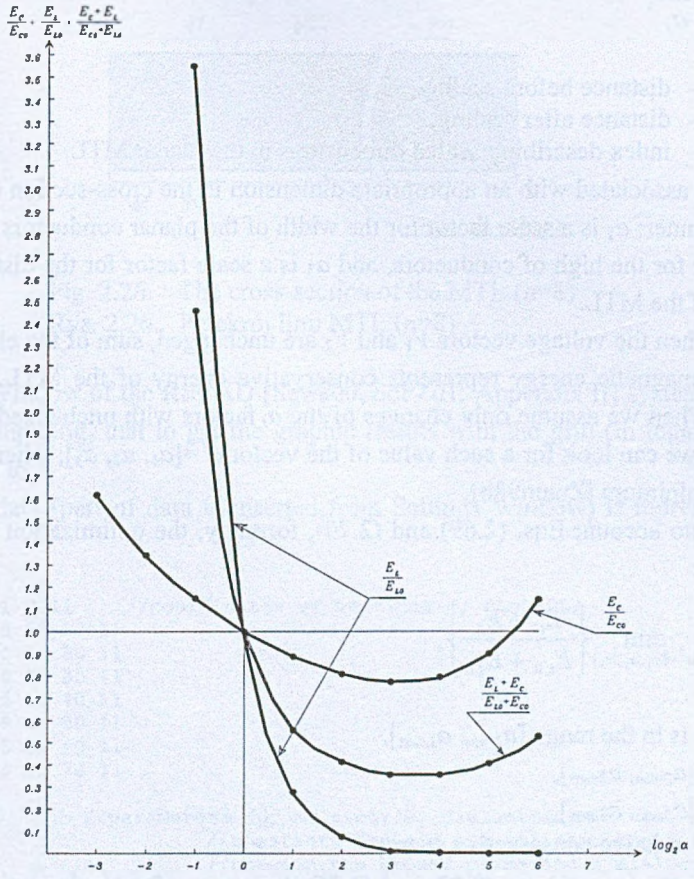


Fig. 2.25. Relative energies E_C/E_{C0}, E_L/E_{L0}, and $(E_C+E_L)/(E_{C0}+E_{L0})$ vs. the scale factor α
Rys. 2.25. Energie względne E_C/E_{C0}, E_L/E_{L0} oraz $(E_C+E_L)/(E_{C0}+E_{L0})$ w funkcji współczynnika skali α

The range of α is between 0.125 and 64. On vertical axis there are values of relative (with respect to E_{C0} and E_{L0}) electrostatic and static magnetic field energies stored in the structure, and relative energy $(E_C+E_L)/(E_{C0}+E_{L0})$ as functions of the scale factor α.

In the presented example, the minimum values of electrostatic energy E_C and conservative energy E_C+E_L were observed for scale factors α =8 and α =11, respectively. The vectors V_1 and V_2 are unchanged during minimization procedure, which is conducted basing on Eq. (2.72).

2.6.3. Scaling of Interconnections – Multi-dimensional Case

Let us introduce a scale factors α_i defined as:

$$D_i^{'} = \frac{D_i}{\alpha_i}, \tag{2.75}$$

where:

D – distance before scaling,
$D_i^{'}$ – distance after scaling,
i – index describing scaled dimensions in the planar MTL.

Index i is associated with an appropriate dimension in the cross-section of the MTL in the following manner: α_1 is a scale factor for the width of the planar conductors of the MTL, α_2 is a scale factor for the high of conductors, and α_3 is a scale factor for the distance between the conductors of the MTL.

In case when the voltage vectors V_1 and V_2 are unchanged, sum of the electrostatic energy and a static magnetic energy represents conservative energy of the MTL. We denote it as $E_{C0} + E_{L0}$. When we assume only changes of the α_i factors with unchanged other parameters of the MTL, we can look for a such value of the vector $\alpha^T=[\alpha_1, \alpha_2, \alpha_3]$, when the conservative energy is at minimum [Znam98b].

Taking into account Eqs. (2.69) and (2.70), formally, the optimization procedure can be expressed by:

$$E_{rel} = \min_{\alpha^T=[\alpha_1,\alpha_2,\alpha_3]} \left\{ \frac{E_C + E_L}{E_{C0} + E_{L0}} \right\}, \tag{2.76}$$

where:

α_1 – is in the range $[\alpha_{1min}, \alpha_{1max}]$,
$\alpha_2 \in [\alpha_{2min}, \alpha_{2max}]$,
$\alpha_3 \in [\alpha_{3min}, \alpha_{3max}]$,
E_{rel} – relative conservative energy.

In optimization procedures (2.72) and (2.76) the ranges of scale factors are constrained to the design rules [Appendix I].

Example 2.8:

We will present the results of energy calculations for a multiconductor transmission line with a cross-section presented in Fig. 2.26 in a certain chip structure [SePZ01]. The length of 8 conductors in perpendicular direction (z-axis direction) to cross-section is l=1cm, and resistance per square is R_S = 0.125Ω/□. The cross-section view of the MTL is presented in Fig. 2.21 (case b), with conductors embedded in air over a silicon substrate (for silicon

$\varepsilon_2 = K_S\varepsilon_0$ with dielectric constant $K_S = 11.7$ and permittivity of vacuum $\varepsilon_0 = 8.854 \cdot 10^{-12}$ F/m). The structure is supplied with two voltage vectors V_1 and V_2 in the following forms:

$V_1^T = [5, 5, 5, 5, 4, 4, 4, 4]$ [V],

$V_2^T = [1, 1, 1, 1, 0.5, 0.5, 0.5, 0.5]$ [V].

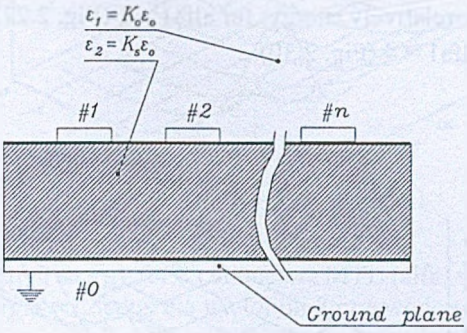


Fig. 2.26. The cross-section of the MTL (n=8)
Rys. 2.26. Przekrój linii MTL (n=8)

In a Settings Window of the KSCAD [Sewe00, SePZ01, Appendix II] system, we declare set of data for computing, that to get the graphic results with the grid (in logarithmic scale with base 2) equal to 1.

Part of input data (part of data is inserted from Settings Window) is represented in the following deck:

```
0 10 5 10 5 11 0 11     //coordinates of vertices of the MTL,
10 10 15 10 15 11 10 11
20 10 25 10 25 11 20 11
30 10 35 10 35 11 30 11
40 10 45 10 45 11 40 11
50 10 55 10 55 11 50 11
60 10 65 10 65 11 60 11
70 10 75 10 75 11 70 11
3 1 11.7 10
                    //parameters for mm program, dielectric
                              //constants for air and silicon, the distance
                              //between the ground plane and a dielectric
                              //interface,
5 5 5 5 4 4 4 4             //voltages.
1 1 1 1 0.5 0.5 0.5 0.5
```

For these data, without scaling (width of conductors) i.e. alfa1=0 (alfa1=$\log_2 \alpha_1$ and α_1=1), the (relative) energy matrix has the form (columns represent alfa2 (high of conductors), and rows - alfa3 (distance between conductors) in the range –1 through 6).

```
1.3934 0.9948 0.7860 0.6818 0.6315 0.6083 0.5999 0.5997
1.4044 1.0000 0.7888 0.6832 0.6321 0.6079 0.5974 0.5943
1.4118 1.0031 0.7906 0.6843 0.6328 0.6082 0.5966 0.5917
1.4158 1.0046 0.7914 0.6848 0.6332 0.6081 0.5961 0.5903
```

```
1.4179 1.0051 0.7916 0.6850 0.6332 0.6080 0.5956 0.5895
1.4170 1.0039 0.7907 0.6843 0.6325 0.6073 0.5948 0.5886
1.4178 1.0045 0.7912 0.6846 0.6328 0.6075 0.5949 0.5885
1.4185 1.0046 0.7911 0.6846 0.6327 0.6074 0.5947 0.5884
```

In the case, when we introduce the scale changing width of lines, high and distance between lines in comparison to the input data, in a graphic form (visualization program in the KSCAD system – Appendix II) we get a set of plots presented in Figs. 2.27 through 2.30. We have accordingly plots for relatively energy: for alfa1 = 1 (Fig. 2.27), for alfa1 = 2 (Fig. 2.28), alfa1=3 (Fig. 2.29), and alfa1 = 4 (Fig. 2.30).

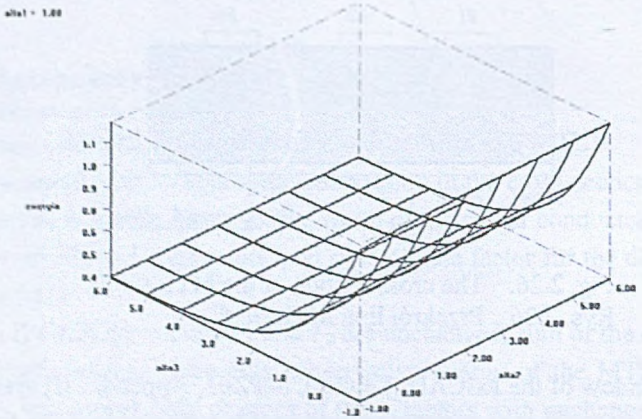


Fig. 2.27. Relative energy for 8 conductors MTL (alfa1=1)
Rys. 2.27. Energia względna dla wielolinii 8 przewodowej (alfa1=1)

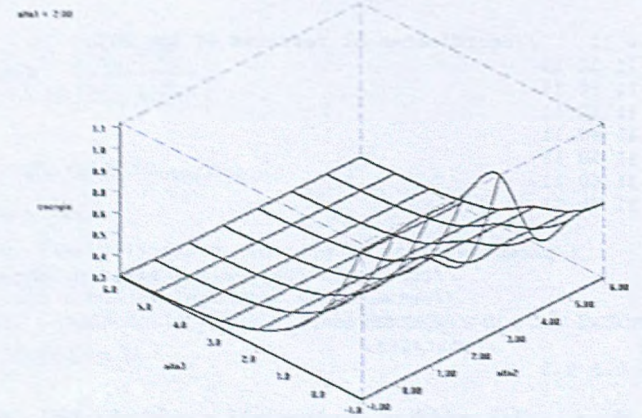


Fig. 2.28. Relative energy for 8 conductors MTL (alfa1=2)
Rys. 2.28. Energia względna dla wielolinii 8 przewodowej (alfa1=2)

Additionally, for this example, in the case non-scaled structure of MTL, we present computed Maxwell's and inductance matrices.

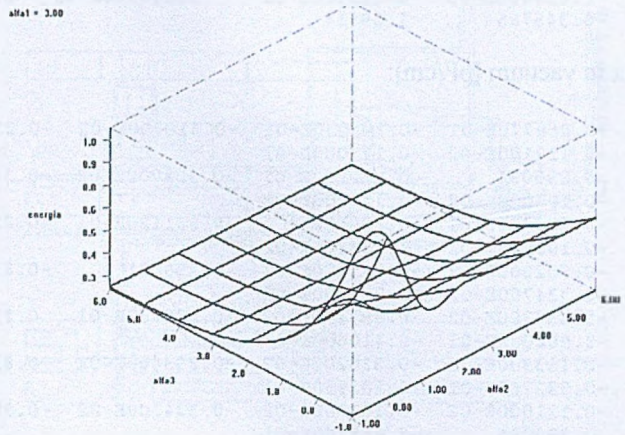


Fig. 2.29. Relative energy for 8 conductors MTL (alfa1=3)
Rys. 2.29. Energia względna dla wielolinii 8 przewodowej (alfa1=3)

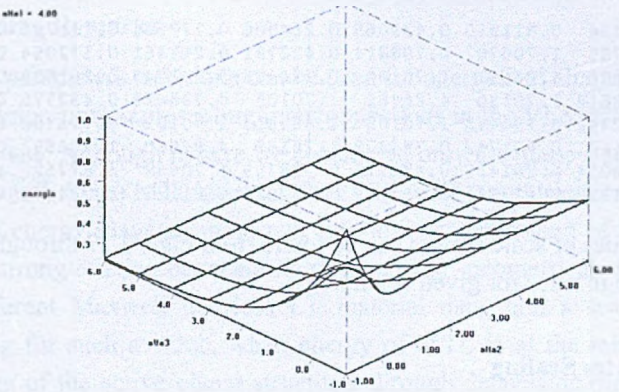


Fig. 2.30. Relative energy for 8 conductors MTL (alfa1=4)
Rys. 2.30. Energia względna dla wielolinii 8 przewodowej (alfa1=4)

Maxwell matrix with dielectric [pF/cm]:

```
 1.59917        -0.345783       -0.211890E-01    -0.424700E-02  -0.198100E-02
-0.125900E-02   -0.888000E-03   -0.791000E-03
-0.345783        1.68663        -0.340605        -0.201920E-01  -0.379600E-02
-0.169900E-02   -0.107200E-02   -0.888000E-03
-0.211890E-01   -0.340605        1.68695         -0.340535      -0.201600E-01
-0.377800E-02   -0.169900E-02   -0.125900E-02
-0.424700E-02   -0.201920E-01   -0.340535         1.68697       -0.340529
-0.201600E-01   -0.379600E-02   -0.198100E-02
-0.198100E-02   -0.379600E-02   -0.201600E-01    -0.340529       1.68697
-0.340535       -0.201920E-01   -0.424700E-02
-0.125900E-02   -0.169900E-02   -0.377800E-02    -0.201600E-01  -0.340535
 1.68695        -0.340605       -0.211900E-01
-0.888000E-03   -0.107200E-02   -0.169900E-02    -0.379600E-02  -0.201920E-01
-0.340605        1.68663        -0.345785
```

```
-0.791000E-03  -0.888000E-03  -0.125900E-02    -0.198100E-02  -0.424700E-02
-0.211900E-01  -0.345785       1.59914
```

and Maxwell matrix in vacuum [pF/cm]:

```
 0.257418      -0.868770E-01  -0.103930E-01  -0.410700E-02  -0.232400E-02
-0.153100E-02  -0.112100E-02  -0.113000E-02
-0.868770E-01   0.290094      -0.832760E-01  -0.902000E-02  -0.334700E-02
-0.183900E-02  -0.121000E-02  -0.112100E-02
-0.103930E-01  -0.832760E-01   0.290522      -0.831120E-01  -0.893400E-02
-0.330200E-02  -0.183900E-02  -0.153100E-02
-0.410700E-02  -0.902000E-02  -0.831120E-01   0.290581      -0.830880E-01
-0.893400E-02  -0.334700E-02  -0.232400E-02
-0.232400E-02  -0.334700E-02  -0.893400E-02  -0.830880E-01   0.290581
-0.831120E-01  -0.902000E-02  -0.410600E-02
-0.153100E-02  -0.183900E-02  -0.330200E-02  -0.893400E-02  -0.831120E-01
 0.290522      -0.832760E-01  -0.103930E-01
-0.112100E-02  -0.121000E-02  -0.183900E-02  -0.334700E-02  -0.902000E-02
-0.832760E-01   0.290094      -0.868760E-01
-0.113000E-02  -0.112100E-02  -0.153100E-02  -0.232400E-02  -0.410600E-02
-0.103930E-01  -0.868760E-01   0.257424
```

and finally, inductance matrix computed from Maxwell matrix in vacuum [nH/cm]:

```
4.95186       1.73454  0.811310 0.439065 0.264806 0.173684 0.121745 0.904018E-01
1.73454       4.87755  1.70670  0.798814 0.432781 0.261461 0.172054 0.121740
0.811310      1.70670  4.86691  1.70190  0.796475 0.431743 0.261458 0.173676
0.439065      0.798814 1.70190  4.86482  1.70105  0.796473 0.432775 0.264789
0.264806      0.432781 0.796475 1.70105  4.86481  1.70189  0.798799 0.439027
0.173684      0.261461 0.431743 0.796473 1.70189  4.86690  1.70668  0.811271
0.121745      0.172054 0.261458 0.432775 0.798799 1.70668  4.87752  1.73446
0.904018E-01 0.121740 0.173676 0.264789 0.439027 0.811271 1.73446  4.95170
```

The optimal values of scale factors can be found from Figs. 2.27 through 2.30 additionally considering the design rules for given technology.

2.6.4. VLSI Gates Scaling

The switching delay in the VLSI gates depends on (among others) the geometrical dimensions of gates (generally depends on technology, gates' power supply, threshold voltage of the gate's transistors, and others). The experimental characterization of the delay times presented here, in the scaled in dimensions, basic VLSI gates is based on the measurements of the delay times in the scaled inverters fabricated in ST2 structure [PiZn94, Appendix I]. Three scaled inverters are designed in the ST2 structure with the layout presented in Fig. 2.31.

The scaling is performed in two directions of the design plane in the same manner. If we described the geometrical dimensions of inverters as 1:2:3, than the delay time t_{dHL} (switching of the inverter output voltage from high to low level) is estimated as 1:1.17:1.44, and delay time t_{dLH} (switching of the inverter output voltage from low to high level) is estimated as 1:1.28:1.78. The contact pads of the tested inverters were excited and loaded with the Fairchild inverters 7404, and the power supply of the ST2 chip was established at 5V. From measurements we can observed for ST2 chip technology, that three times decreasing of dimensions leads to nearly two times faster inverter gate.

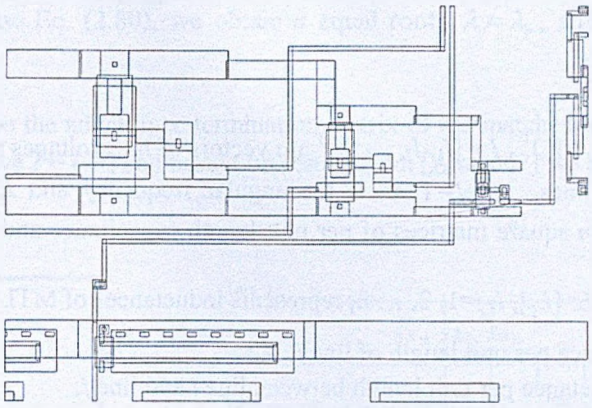


Fig. 2.31. Layout of the scaled VLSI inverters (part of the ST2 structure)
Rys. 2.31. Struktury skalowanych inwerterów VLSI (fragment struktury ST2)

2.6.5. Concluding Remarks

The extraction parameters technique can be used for energetical characterization of multiconductor transmission lines representing interconnections in the VLSI/ULSI structures when the scaling takes place. Although in here we considered only the quasi-static case, the conclusions are more general. Since MTL working in VLSI/ULSI structures have to be all time recharged, the static energy plays an important role in a proper design of MTL for small geometries due to a strong relation between the static energy, geometrical shape of conductors' cross-section (different Maxwell matrices C), material data, and a scaling factor can be applied for looking for such a value, when energy of MTL is at the minimum for a given technology. Scaling of the active planar structures through decreasing dimensions, increases the speed of switching (e.g. from measurements we can observed, that three times decreasing of dimensions on the design plane, leads to nearly two times faster inverter gate).

2.7. Matching

Design of fast switching MTL interconnects in a VLSI structures requires proper termination of the MTL to avoid reflections decreasing the speed of transmission. Here, we will discuss two approach to this problem: matching the end of MTL using the termination network [Amem67] and more practical from designer's point of view, the method of so called diagonal matching [ZnPS99].

Let us consider the model of interconnects as a system of n parallel, lossless transmission lines and a ground, in the homogeneous and isotropic medium, in the form of the matrix telegrapher's equations

$$\frac{d}{dz}V = -j\omega LI \tag{2.77}$$

$$\frac{d}{dz}I = -j\omega CV, \tag{2.78}$$

where, $V = [V_1, V_2, \ldots, V_n]^T$, $I = [I_1, I_2, \ldots, I_n]^T$ are vectors of line voltages and currents, z is the distance along the lines, $j = \sqrt{-1}$, ω is the angular frequency and L, C are symmetric, positive definite, $n \times n$ square matrices of per unit length capacitance and inductance, respectively.

In (2.77) matrix $L=[L_{ij}]$, $i,j=1, 2, \ldots n$, represents inductances of MTL where:

L_{ii} – self inductance per unit length of line i,
L_{ij} – mutual inductance per unit length between line i and line j,
$L_{ij} = L_{ji}$.

In (2.78), the Maxwell matrix $C=[C_{ij}]$, $i,j=1, 2, \ldots n$, basing on the theorem (p. 2.5.3) can be expressed by the elements of the "two-terminal" capacitance matrix $T=[T_{ij}]$ (Eq. 2.10) in the form:

$$C = \begin{bmatrix} \sum_{i=1}^{n} T_{1i} & -T_{12} & -T_{13} & \cdots\cdots & -T_{1n} \\ -T_{21} & \sum_{i=1}^{n} T_{2i} & -T_{23} & \cdots\cdots & -T_{2n} \\ -T_{31} & -T_{32} & \sum_{i=1}^{n} T_{3i} & \cdots\cdots & -T_{3n} \\ \vdots & \vdots & \vdots & & \vdots \\ -T_{n1} & -T_{n2} & -T_{n3} & \cdots\cdots & \sum_{i=1}^{n} T_{ni} \end{bmatrix} \tag{2.79}$$

The elements T_{ij} in (2.79) represent the capacitances of MTL where:

T_{ii} – capacitance per unit length between line i and ground,
T_{ij} – capacitance per unit length between line i and line j, $i \neq j$ and $i,j=1, 2, \ldots n$,
$T_{ij} = T_{ji}$.

The propagation velocities associated with propagation modes in the MTL can be found from the eigenvalues of the matrix LC [Amem67]. Solving equation:

$$|\lambda U - LC| = 0, \tag{2.80}$$

where

U – a unit matrix,

generally, n values of $v = \sqrt{\lambda}$ are obtained (v denotes propagation velocity). However, if we consider homogeneous and isotropic medium all propagation velocities coincide, and the eigenvalues are the same. This takes place when

$$LC = \lambda_p U. \tag{2.81}$$

Solving in this case Eq. (2.80), we obtain n equal roots $\lambda = \lambda_p$, and common velocity $v_p = 1/\sqrt{\lambda_p}$.

Let us denote G be the admittance termination matrix of the matched load network. Then from Fig. 2.32a we have $I = GV$, and basing on results from [Amem67] we have:

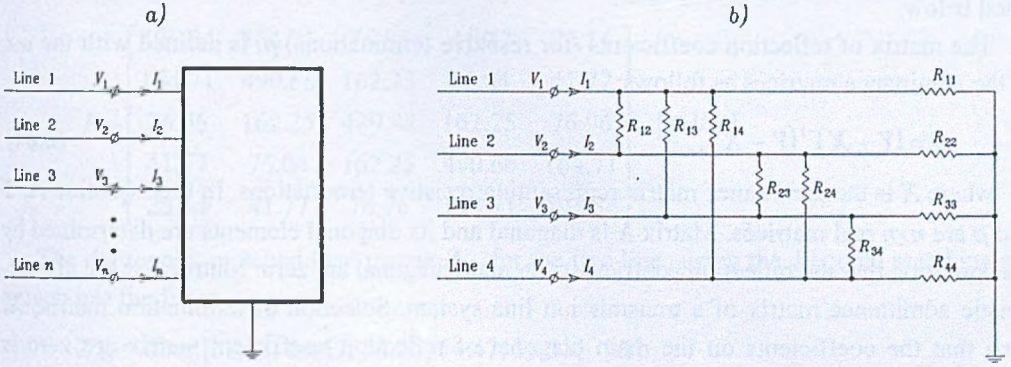


Fig. 2.32. Matched termination of MTL: a) matched termination for a system of n parallel lines and a ground, b) matched termination network for four lossless MTL

Rys. 2.32. Terminatory dopasowania dla MTL: a) dla systemu n równoległych przewodów i ziemi, b) terminator bezstratnej linii czteroprzewodowej

$$G = \begin{bmatrix} \sum_{i=1}^{n} \frac{1}{R_{1i}} & -\frac{1}{R_{12}} & -\frac{1}{R_{13}} & \cdots & -\frac{1}{R_{1n}} \\ -\frac{1}{R_{21}} & \sum_{i=1}^{n} \frac{1}{R_{2i}} & -\frac{1}{R_{23}} & \cdots & -\frac{1}{R_{2n}} \\ -\frac{1}{R_{31}} & -\frac{1}{R_{32}} & \sum_{i=1}^{n} \frac{1}{R_{3i}} & \cdots & -\frac{1}{R_{3n}} \\ \vdots & \vdots & \vdots & & \vdots \\ -\frac{1}{R_{n1}} & -\frac{1}{R_{n2}} & -\frac{1}{R_{n3}} & \cdots & \sum_{i=1}^{n} \frac{1}{R_{ni}} \end{bmatrix}, \tag{2.82}$$

where:

R_{ii} – resistance between line i and ground, i=1, 2, ... n,

R_{ij} – resistance between line i and line j, $i \neq j$ and i, j=1, 2, ... n,

R_{ij}=R_{ji}, and i, j=1, 2, ... n,

and

$$R_{ij} = \frac{1}{v_p T_{ij}}, \qquad i, j = 1, 2, 3, \ldots, n. \tag{2.83}$$

The example of matched termination network for 4-line MTL is presented in Fig. 2.32b.

The cases when propagation velocities do not coincide are also discussed in [Amem67].

In the design of MTL in VLSI structures, the nice results obtained by Amemyia have a minor meaning. In these structures, each line is terminated by an active circuit which has no direct connections to other terminating circuits, and ideal matching in the case of coupled lines is not possible. Therefore, the design engineers practice so called diagonal matching defined below.

The matrix of reflection coefficients (for resistive terminations) ρ, is defined with the use of the admittance matrices as follows:

$$\rho = (Y + X)^{-1}(Y - X), \tag{2.84}$$

where X is the admittance matrix representing resistive terminations. In this equation X, Y and ρ are $n \times n$ real matrices. Matrix X is diagonal and its diagonal elements are determined by the condition that the reflection coefficients on main diagonal are zero. Matrix Y is the characteristic admittance matrix of a transmission line system. Selection of termination matrix, X, such that the coefficients on the main diagonal of reflection coefficient matrix are zero is called diagonal matching.

The numerical algorithm for computation of characteristic admittance matrix of the telegrapher's equations in (2.84) is presented in [SzPa99], the iterative algorithm of determination of the matrix X such that the coefficients on the main diagonal of reflection coefficient matrix ρ are zero and diagonally matched load matrix Z_{dm} is presented in [ZnPS99, YoPS99], and the convergence analysis of this algorithm is proven in [SzPa94].

Example 2.9: Diagonal matching.

Using diagonal matching method, we will find the diagonally matched load matrix Z_{dm} for the prototypical interconnect system presented in Fig. 2.33.

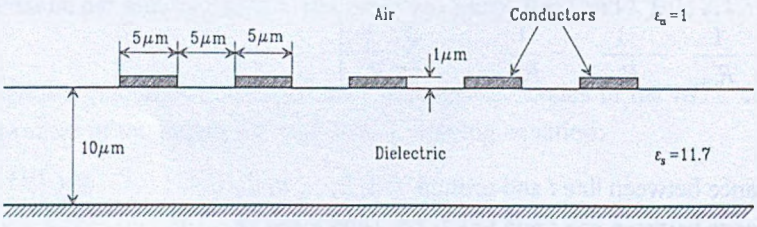


Fig. 2.33. Geometry of the microstrip lines (Example 2.9)
Rys. 2.33. Geometria wielolinii transmisyjnej (przykład 2.9)

The capacitance and inductance matrices of idealized model of these lines have the following forms [ZnPS99, YoPS99]:

$$C = \begin{bmatrix} 140.17 & -30.79 & -1.91 & -0.38 & -0.19 \\ -30.79 & 153.67 & -30.51 & -1.86 & -0.38 \\ -1.91 & -30.51 & 153.69 & -30.51 & -1.91 \\ -0.38 & -1.86 & -30.51 & 153.67 & -30.79 \\ -0.19 & -0.38 & -1.91 & -30.79 & 140.17 \end{bmatrix} \quad [\text{pF/m}]$$

$$L = \begin{bmatrix} 497.84 & 164.71 & 76.96 & 41.77 & 25.54 \\ 164.71 & 490.66 & 162.25 & 76.04 & 41.77 \\ 76.96 & 162.25 & 489.48 & 162.25 & 76.96 \\ 41.77 & 76.04 & 162.25 & 490.66 & 164.71 \\ 25.54 & 41.77 & 76.96 & 164.71 & 497.84 \end{bmatrix} \quad [\text{nH/m}]$$

The diagonally matched load matrix Z_{dm} for the five lines using the diagonal matching approach has the form:

$$Z_{dm} = diag\ [58.33, 54.47, 54.25, 54.47, 58{,}33] \quad [\Omega].$$

It is worth noting the variation of matched impedance with the position in the structure. This gives suggestion for designing of receivers' input impedance for diagonal match.

2.8. Losses in Dielectrics

The switching transients in a high-speed planar VLSI structures depend on dielectric properties of substrate under the signal and ground microstrip lines. Most important for transient analysis is recharging of dielectrics which depends on capacitance of a microstrip line that recharges due to dielectric absorption phenomenon. One can simulate the process using circuit simulators (like SPICE [VZNP81]) after identification of the proper model.

We will discuss an implementation of a microstrip line dielectric absorption model in a form of RC elements chain, and present a method of parameter identification based on the exponential approximation [Znam97]. Presented algorithm is implemented to the identification of the model based on the data gathered from the measurements of a stimulated planar microstrip line (test structure ST2 – Appendix I).

2.8.1. Model of a Dielectric Absorption

We consider a microstrip line and a ground conductor on a substrate shown in Fig. 2.34. The losses like microstrip line resistance and leakage resistance can be easily taken into account in developing a circuit simulation model describing a microstrip. More important issue is implementation of capacitance and effects of dielectric internal losses into the model.

It is well-known that the dielectric constant of solids depends on frequency [Cole41] and can be presented as a complex function in a simplest form:

$$\varepsilon^* = \varepsilon_\infty + \frac{\varepsilon_0 - \varepsilon_\infty}{1 + j\omega\tau_0}. \tag{2.85}$$

In the Eq. (2.85) ε_∞ is the infinite frequency dielectric constant, ε_0 is the zero frequency (static) dielectric constant, and τ_0 is the relaxation time. This "relaxation" of dielectric takes place since the activation-energy thresholds delay the dielectric polarization associated with capacitor (i.e. the microstrip line and the ground) voltage changes and thus cause frequency-dependent energy dissipation which can be referred to as microstrip/ground dielectric absorption. Due to results of conducted measurements [Cole41, Dow58], ε_∞ was small compared to ε_0 and therefore instead of Eq. (2.85), the microstrip/ground dielectric absorption phenomenon can be more accurately described by a set of fixed leakage resistances R_1, R_2,..., R_n in series with small capacitances C_1, C_2, ... , C_n respectively (Fig. 2.35). The set is known as the Dow's model [Dow58]. Values of n as small numbers have been used (e.g. II order approximation has n=2).

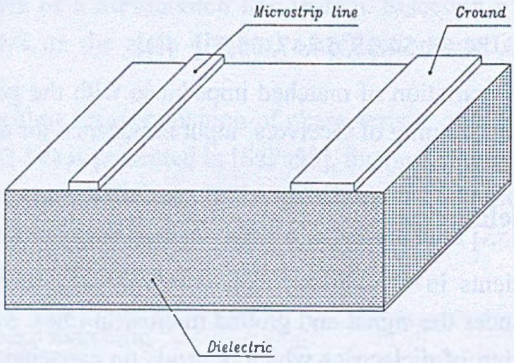


Fig. 2.34. A microstrip line and a ground conductor on a substrate
Rys. 2.34. Mikrolinia i przewód ziemi na podłożu

Since the application of Eq. (2.85) for developing transient-analysis model is inconvenient, we will use Dow's model to describe a segment of microstrip line, assuming its length equal l. In the equivalent circuit in Fig. 2.35 representing the dielectric absorption model, symbols R_1, C_1, R_2, C_2, ... , R_n, C_n denotes absorption elements of a microstrip per l length.

It is clear that in order to identify absorption elements for a segment k-times shorter than l, we have to multiply R_i by k and divide C_i by k so in the further discussion we will not take the length of the microstrip line into consideration.

Let's assume, that the microstrip line was stimulated by the unity-step voltage with the amplitude V_β. Currents flowing through the elements in the model are given by:

$$i_m = \sum_{k=1}^{n} i_k = \sum_{k=1}^{n} \frac{V_\beta}{R_k} e^{-\frac{t}{R_k C_k}}, \tag{2.86}$$

where i_m is the total current from a source flowing through the dielectric, and i_1, i_2, ... i_n are the currents in branches (R_1, C_1), (R_2, C_2), ... , (R_n, C_n) respectively.

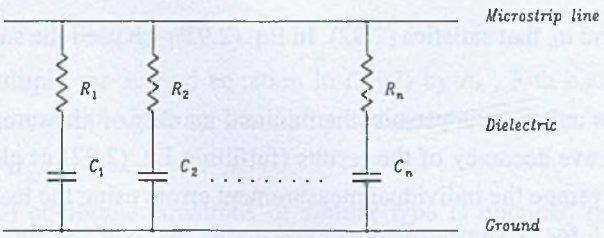


Fig. 2.35. The microstrip line dielectric absorption model
Rys. 2.35. Model absorpcji dielektrycznej podłoża dla mikrolinii

On the other hand, we drew a conclusion from the observations that the dielectric current has a transient-time form similar to a sum of exponents. Assuming that the measured current has a following form:

$$i = \sum_{k=1}^{n} I_k e^{-\frac{t}{T_k}}, \tag{2.87}$$

for a given V_β, we can find from Eqs. (2.86) and (2.87) parameters of the model (Fig. 2.35) if we determine the coefficients I_k and T_k for a current i which is given, as a measured function of the time t.

2.8.2. Identification Algorithm

We consider a measured current i as a time function $i=A(t)$. The function $A(t)$ may be approximated by a function $f^*(t)$:

$$A(t) \approx f^*(t), \tag{2.88}$$

where the function $f^*(t)$ has a form of finite sum of exponents:

$$f^*(t) = I_1 e^{-\frac{t}{T_1}} + I_2 e^{-\frac{t}{T_2}} + \cdots + I_n e^{-\frac{t}{T_n}}, \tag{2.89}$$

where I_k, T_k are constants. If the measurements are realized in N equally spaced points of time, and the single time interval is determined as Δt, then the function $A(t)$ can be characterized by the set of values A_k:

$$A_k = A(k\Delta t), \tag{2.90}$$

where k=0, 1, 2, ... , N–2, N–1, since

$$t = k\Delta t. \tag{2.91}$$

From Eqs. (2.88), (2.89) and (2.91) we have:

$$f^*(k\Delta t) = f(t) \approx A_k. \tag{2.92}$$

Therefore, the problem of finding approximation of the function $A(t)$ by a function (2.89) i.e. finding the values I_i and T_i (i=1, 2, ... , n) is reduced to the task:

for a set of measurements A_k (k=0, 1, 2, ... , N–2, N–1), find the function

$$f(k)=\sum_{i=1}^{n} I_i e^{a_i k} \ , \tag{2.93}$$

for such I_i and a_i, that satisfies (2.92). In Eq. (2.93), we used the substitution

$$-\Delta t/T_i = a_i. \tag{2.94}$$

To determine $2n$ unknown constants, the minimal number of measurements have to be $2n$ but in order to improve accuracy of the results (fulfilling Eq. (2.92) as close as possible), we can use $N>2n$ and average the individual measurement errors using the least-squares method.

To find a_i and I_i for N values of measurements A_k, we will use the Prony's method described in [Hild56].

We rewrite Eq. (2.93) in more convenient way, replacing:

$$e^{a_i} = \mu_i \ . \tag{2.95}$$

Thus

$$f(k) = I_1\mu_1^k + I_2\mu_2^k + \cdots + I_n\mu_n^k \ , \qquad (k = 0, 1, 2, \ldots, N-1). \tag{2.96}$$

Basing on Eq. (2.92) and approximating $f(k)$ with A_k, from Eq. (2.96) we have:

$$\begin{aligned} I_1 + I_2 + \ldots\ldots + I_n &= A_0 \\ I_1\mu_1 + I_2\mu_2 + \ldots\ldots + I_n\mu_n &= A_1 \\ &\vdots \\ I_1\mu_1^{N-1} + I_2\mu_2^{N-1} + \ldots\ldots + I_n\mu_n^{N-1} &= A_{N-1} \end{aligned} \tag{2.97}$$

If we introduce substitutions:

$$I^{\mathrm{T}} = [I_1, I_2, \ldots, I_n],$$

$$V^{\mathrm{T}} = [A_0, A_1, \ldots, A_{N-1}],$$

$$M = \begin{bmatrix} 1 & 1 & \ldots & 1 \\ \mu_1 & \mu_2 & \ldots & \mu_n \\ \mu_1^2 & \mu_2^2 & \ldots & \mu_n^2 \\ \vdots & \vdots & \vdots & \vdots \\ \mu_1^{N-1} & \mu_2^{N-1} & \ldots & \mu_n^{N-1} \end{bmatrix}$$

where index T designates vector transposition, we can write Eq. (2.97) in the form:

$$M\,I = V. \tag{2.98}$$

From Eq. (2.98) the n unknown I_1, I_2, ... , I_n could be solved exactly if N=n or approximately if N>n by the least-squares method [Hild56, Manc71]. For this solution, values of μ_1, μ_2, ... , μ_n have to be known (or preassigned). However, if the μ_1, μ_2, ... , μ_n are also to be determined, at least $2n$ equations are needed (N≥$2n$). Let μ_i be the roots of the algebraic equation

$$\mu^n - \alpha_1\mu^{n-1} - \alpha_2\mu^{n-2} - \ \ldots \ - \alpha_{n-1}\mu - \alpha_n = 0. \tag{2.99}$$

In order to determine the coefficients α_i, we will use Eq. (2.97). We multiply the first equation in (2.97) by α_n, the second equation by α_{n-1}, ... , the n-th by α_1 and $(n+1)$-th by 1 and after adding up the results, we obtain:

$$A_n - \alpha_1 A_{n-1} - \ \dots \ - \alpha_n A_0 = 0 . \tag{2.100}$$

And next we multiply the second equation in (2.97) by α_n, 3-th equation by α_{n-1}, ... , $(n+1)$-th equation by α_1 and $(n+2)$-th by 1 and after adding up the results, we obtain:

$$A_{n+1} - \alpha_1 A_n - \alpha_2 A_{n-1} - \ \dots \ - \alpha_n A_1 = 0 . \tag{2.101}$$

A set of $N-(n+2)$ additional equations of similar type is obtained in the same way by starting successively with third, forth , ... , $(N-n)$-th equations.

So we find the $N-n$ linear equations:

$$A\alpha = W , \tag{2.102}$$

where

$$\alpha^{\mathrm{T}} = [\alpha_1, \alpha_2, \ \dots \ , \alpha_n],$$
$$W^{\mathrm{T}} = [A_n, A_{n+1}, \ \dots \ , A_{N-1}],$$

and a matrix A:

$$A = \begin{bmatrix} A_{n-1} & A_{n-2} & \dots & A_0 \\ A_n & A_{n-1} & \dots & A_1 \\ \vdots & \vdots & \dots & \vdots \\ A_{n-2} & A_{n-3} & \dots & A_{N-(n+1)} \end{bmatrix} .$$

If $N=2n$, the set of Eqs. (2.102) can be solved directly; if $N>2n$, a least-squares solution can be found. Once the coefficients α are found, the μ_i are determined by solving Eq. (2.99). Then the I can be found from Eq. (2.98) and using (2.95) and (2.94) for given Δt we will find T_i $(i=1, 2, \dots , n)$.

We do not consider cases, when the roots of Eq. (2.99) are not real or positive because of physical interpretation of such results (see the developed model). Error analysis of the technique described has been presented in [Hild56].

Summarizing, the process of identification of the dielectric absorption model parameters for the microstrip line, can be gathered in a form of the following algorithm:

Algorithm DIELECTRIC-ABSORPTION-MODEL-IDENTIFICATION (DAMI)

- Given:
  - n - order of the approximation of the function $A(t)$,
  - $V^{\mathrm{T}} = [A_0, A_1, \dots , A_{N-2}, A_{N-1}]$ - vector of measurements and $N > 2n$,
  - Δt - time interval.
- Build the vector W and the matrix A.
- Solve Eq. (2.102) for a vector α using the least-squares method:

$$\alpha = (A^{\mathrm{T}} A)^{-1} A^{\mathrm{T}} W . \tag{2.103}$$

- Solve Eq. (2.99) using elements of the vector α as coefficients. If roots of Eq. (2.99) are not real and positive decrease the order of approximation n, and start the algorithm again.
- For found μ_i (i=1, 2, ... , n), build the matrix M and solve Eq. (2.98) for vector I using the least-squares method:

$$I = (M^T M)^{-1} M^T V. \tag{2.104}$$

- Using Eqs. (2.95) and (2.94) find T_i:

$$T_i = -\frac{\Delta t}{\ln \mu_i}. \tag{2.105}$$

- Using T_i, I, V_β, Eqs. (2.86) and (2.87), find:

$$R^T=[R_1, R_2, \ldots, R_n], \text{ and } C^T=[C_1, C_2, \ldots, C_n]. \tag{2.106}$$

2.8.3. Measurements

The algorithm DAMI was implemented in a program DIELEK [Appendix II] for the microstrip line dielectric absorption model of microstrip, designed in a test structure ST2 (CIF description enclosed in Appendix I). The layout view of structure is shown in Fig. 2.36.

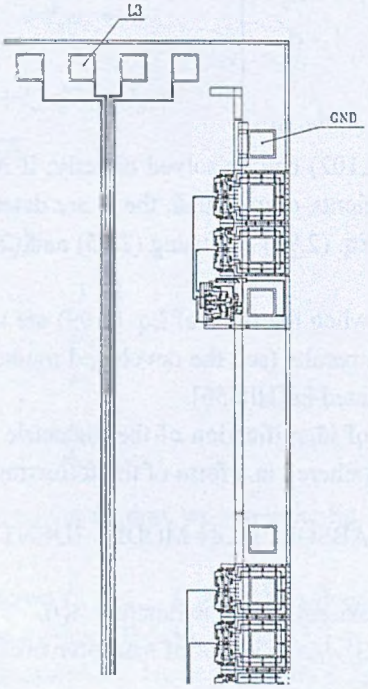


Fig. 2.36. The microstrip line (L3) and a ground (GND) on the ST2 test structure
Rys. 2.36. Mikrolinia (L3) oraz ziemia (GND) w strukturze testowej ST2

The measurements were performed for the microstrip line pad L3 and a ground pad GND. The measurement circuit with the probe and the input of digitizing/storage HP 54601A oscilloscope [HePa92] is presented in Fig. 2.37. The dielectric current i was measured indirectly (Table 2.5), as a voltage drop U_p (data for the DIELEK program) on a precise resistor R_p=96Ω.

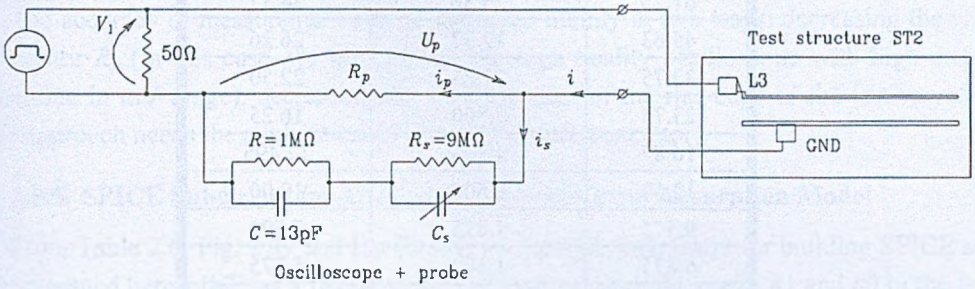


Fig. 2.37. The measurement circuit
Rys. 2.37. Schemat układu pomiarowego

The pad L3 was stimulated from a pulse generator class of HP 8082A [Agil01] matched with the 50Ω load resistance and a pulse amplitude equal 4.344V. The generator transition time was approximately 4ns (the first values of U_p and B (t=0 ns) in Table 2.5, result from fitting the transients of U_p and B voltages in the time interval after t=0ns), and the pulse duration was long enough to charge and discharge the dielectric.

The parasitic capacitances of package and external wiring (background current measured as a voltage drop B on a precise resistor R_p) are eliminated by double measurement: complete IC including die with the microstrip line, and package with the die removed. It is important to perform the double measurement without changing the external wiring for accurate background current elimination. For this reason all wiring should be rigid to minimize changes which would reduce the effectiveness of background parasitic reduction. The results from the DIELEK program for n=2, N=17 and Δt=10ns, are shown in Table 2.6.

2.8.4. Error Evaluation

From the measurement circuit (Fig. 2.37) we see, that important source of error is the impedance Z_s in a branch with current i_s. The probe parameters was tuned basing on the HP 54601A oscilloscope reference pulse source (1.2kHz, 5V) but depending on frequency, the $|Z_s|$ is changing in comparison with R_p.

Thus, the estimated error of the current measurement is expressed by

$$\delta = \left|\frac{i_s}{i}\right|; \qquad i = i_s + i_p,$$

where i_p, i_s, i are currents shown in Fig. 2.37.

Table 2.5

Transient state of voltage U_p and background voltage B with sampling interval Δt=10ns

U_p [mV]	Background (B) [mV]	U_p–B [mV]
103.8	46.00	57.80
61.25	26.88	34.37
45.63	19.37	26.26
33.75	11.25	22.50
23.75	7.500	16.25
16.87	4.375	12.495
12.50	2.500	10.00
9.375	1.875	7.500
6.875	1.100	5.775
5.000	0.625	4.375
3.750	0.312	3.438
2.500		2.500
2.240		2.240
1.875		1.875
1.250		1.250
1.000		1.000
0.625		0.625

After calculations we get:

$$\delta = \frac{R_p[T^2 + (RC)^2]}{\sqrt{[R_p T^2 + R_p (RC)^2 + 10RT^2]^2 + (10R)^2 T^2 (RC)^2}},$$

where T is the approximated time constant of the current i transient.

Table 2.6

Identified time constants

Δt [ns]	Currents [nA]	Time constants [ns]
10	I_1 = 149.954 I_2 = 452.102	T_1 = 2.84001 T_2 = 41.0801

For the conditions of measurement (T = 26ns) we get δ = 0.48%. The error in determining the values of resistances R_1 and R_2 in the dielectric absorption model is the same as estimated current error. The evaluation of the error in determining the time constants T_1 and T_2 gives not

worse than 2.8% error estimation (error propagation in the time constants calculation based on the current measurements data, small changes of the voltage drop on the dielectric during the measurement, and slight irregularities at the borders of the tested dielectric).

The sensitive dependency of the time constants T_1 and T_2 on the $(U_p–B)$ voltage changes near the 57.8mV (t=0 ns) is small: we have for +3% and –3% changes of $(U_p–B)$, the changes of +1.8% and –4.0% for time constants T_1, and +0.39% and –0.48% for time constants T_2 respectively.

The accuracy of measurement can be improved mainly in two ways: decreasing the value of resistor R_p (in this case, we have to use the high quality oscilloscope with high display resolution in mV range), decreasing the transient time of the rise edge of the test waveform (this approach needs the application of a very fast pulse generator).

2.8.5. SPICE Subcircuit for Microstrip Line Dielectric Absorption Model

From Table 2.6, Fig. 2.37 and Eq. (2.106) we find all parameters for building SPICE subcircuit named here LINE, as a two-terminal network between the nodes #1 and #0 in the form which can be used in the SPICE simulator as a II order microstrip line dielectric absorption model of the microstrip L3 in the structure ST2:

```
*MICROSTRIP LINE L3 DESCRIPTION
.SUBCKT LINE 1
R1 1 2 28.5835 K
C1 2 0 0.0993584 P
R2 1 3 9.48061 K
C2 3 0 4.33306 P
.ENDS LINE
```

2.8.6. Switching Transients in the Presence of Dielectric Absorption

In VLSI and particularly ULSI structures, the microstrip line losses expressed by dielectric absorption phenomenon, can be serious source of structure switching speed degradation. We illustrate these effects by simulation using the data for microstrip line description from measurement performed in test structure and identification of model parameters. We will build the model of transmission system containing identical driver and loaded receiver gates, and a model of microstrip line using the SPICE [QNPS93, VZNP81, Nage75] simulator. The goal of simulation is to verify the switching parameters like transition and delay times in dependency on length of microstrip line with the dielectric absorption effect, connecting a CMOS driver and receiver gates which have been design in a small geometry.

The data describing dielectric absorption in microstrip line, were found in experiment [Znam97] on test structure ST2 (Appendix I). As a line driver and receiver will be used inv_min inverter (complement operation) designed in LOCOS CMOS technology (λ=1.5μm) presented in Fig. 2.38a. To improve readability of structure draw, the layout is presented in groups of layers (Fig. 2.38b, 2.38c, and 2.38d). CIF description of inv_min can be found in Appendix I, p. 6.1.3. We will simulate behavior of a such transmission system using gates with minimal dimensions i.e. as small as possible, however fulfilling the design rules for this

process [Grod93]. The input signal to the driver's inverter is connected in polysilicon (wire numbered 2, (0, 37λ) – Fig. 2.38), yet the output signal from driver in poly layer (wire #3, (18λ, 37λ)), through contact (CONT) is connected to the metal one (MET1) layer and the first wire of the transmission line microstrip.

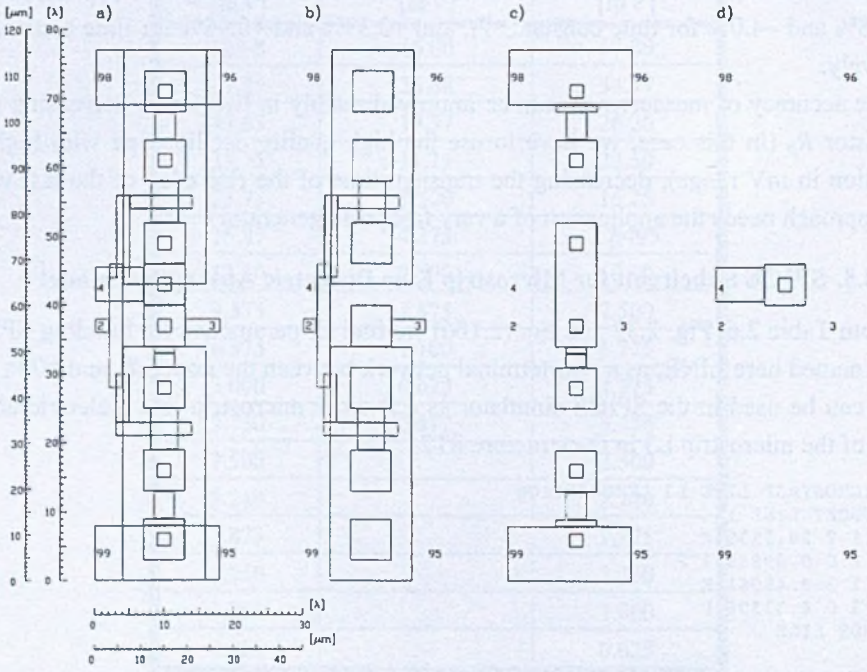


Fig. 2.38. Inverter inv_min CMOS: a) all design layers, b) PWE, NWE, POA, NOA, POLY layers, c) CONT, MET1 layers, d) VIA, MET2 layers. Dimensions are in µm and design units λ=1.5µm

Rys. 2.38. Inwerter inv_min CMOS: a) wszystkie warstwy projektowe, b) PWE, NWE, POA, NOA, POLY, c) CONT, MET1, d) VIA, MET2. Wymiary w µm oraz w jednostkach projektowych λ=1.5µm

The second wire of transmission line is a global GND wire shunting ground lines from the driver gate (route #95) and receiver gate (route #95 respectively). The output signal from transmission line (metal one) through contact (CONT) is routed to poly at the input of receiver inverter (wire #2). Routes #98 in driver and receiver gates are supplied by the voltage V_{DD}.

Layout of the system is presented in Fig. 2.39.

Symbol L describes the length of transmission line and D is equal to the distance of metal lines in tested structure ST2. For simplification, we neglect the influence of short leads of signal and ground lines in the discussed gates.

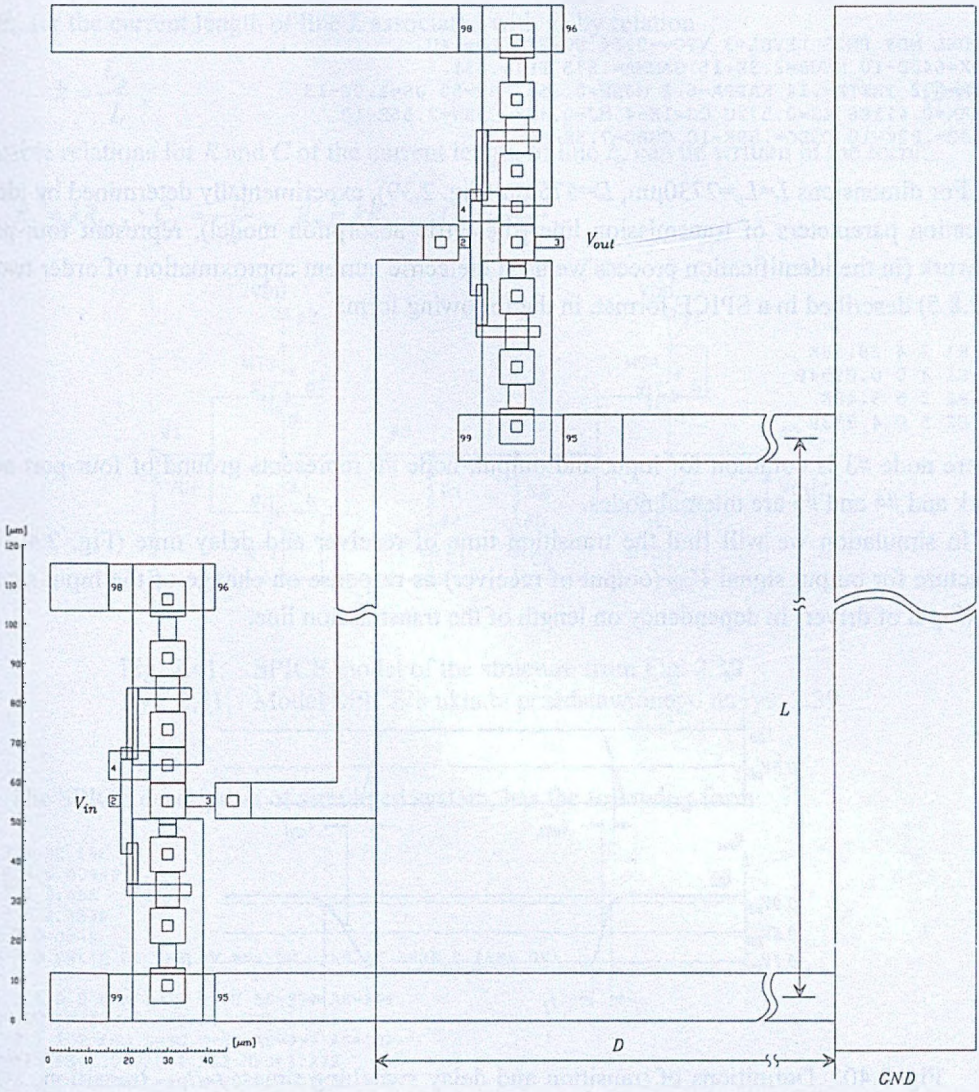


Fig. 2.39. Mask of a system including the inv_min inverter of the driver, inv_min inverter of the receiver, and the transmission line of length L with dielectric losses

Rys. 2.39. Maska systemu zawierającego inwerter inv_min nadajnika, inwerter inv_min odbiornika oraz linię transmisyjną długości L ze stratami dielektryka

The transistor's SPICE models (LEVEL=3) for gates, delivered by Silicon Foundry describe the following .MODEL [Foty97, Aror92] commands:

```
.MODEL MDN NMOS LEVEL=3 VTO=0.85 UO=6.1E2 LD=.35U
+TOX=640E-10 NSUB=8.4E15 GAMMA=1.9 PHI=.686
+ETA=1.11 THETA=.02 KAPPA=2.0 MJSW=0.323 RSH=30 JS=1.E-12
+VMAX=.137E6 XJ=.572U CJ=3.68E-4 MJ=.4 CJSW=5.66E-10
+CGSO=.89E-10 CGDO=.89E-10 CGBO=7.5E-10
```

```
.MODEL MDP PMOS LEVEL=3 VTO=-0.54 UO=220 LD=.4U
+TOX=640E-10 NSUB=2.9E+15 GAMMA=.575 PHI=.631
+ETA=0.2 THETA=.14 KAPPA=6.2 MJSW=0.256 RSH=50 JS=1.0E-13
+VMAX=0.411E6 XJ=0.572U CJ=1E-4 MJ=0.455 CJSW=2.56E-10
+CGSO=.89E-10 CGDO=.89E-10 CGBO=7.5E-10
```

For dimensions $L=L_p=2730\mu m$, $D=575\mu m$ (Fig. 2.39), experimentally determined by identification parameters of transmission line (dielectric absorption model), represent four-port network (in the identification process we used dielectric current approximation of order two – p. 2.8.5) described in a SPICE format, in the following form:

```
R1 3 4 28.58K
C1 4 0 0.0994P
R2 3 5 9.48K
C2 5 0 4.333P
```

where node #3 is common for input and output, node #0 represents ground of four-port network and #4 and #5 are internal nodes.

In simulation we will find the transition time of receiver and delay time (Fig. 2.40) in structure for output signal V_{out} (output of receiver) as response on change of the input signal V_{in} (input of driver) in dependency on length of the transmission line.

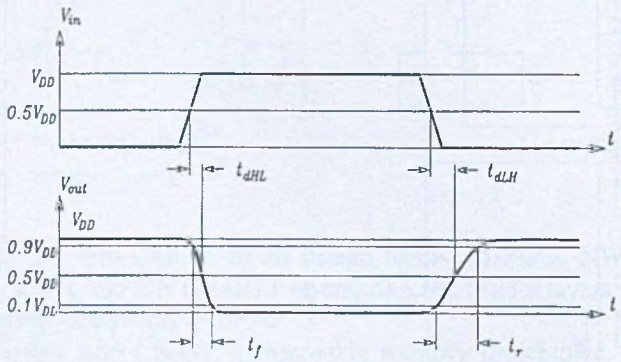


Fig. 2.40. Definitions of transition and delay switching times: t_f, t_r – transition times (fall time and rise time respectively), t_{dHL}, t_{dLH} – delay times

Rys. 2.40. Definicja czasów przełączania: t_f – czas opadania, t_r – czas narastania, t_{dHL}, t_{dLH} – czasy opóźnienia

Input signal has a rise and fall times equal 1ns for level change 5V. The width of input pulse must be enough large to make observable full transient state of output signal. For transition and delay times measurements we will use proper options of simulator (e.g. CURSOR and RANGE options for simulator Pspice [MicS89, Tuin95].

The diagram of simulated system in SPICE format is presented in Fig. 2.41. We can see, if measured R, C parameters of the line of length L_p yield

$$R_{1p}=28.58k\Omega, \quad R_{2p}=9.48k\Omega, \quad C_{1p}=0.0994pF, \quad C_{2p}=4.333pF, \tag{2.107}$$

then, for the current length of line L associated with L_p by relation

$$k = \frac{L_p}{L}, \tag{2.108}$$

suitable relations for R and C of the current length of line L, can be written in the form:

$$R_1 = kR_{1p}, \quad C_1 = \frac{C_{1p}}{k}, \quad R_2 = kR_{2p}, \quad C_2 = \frac{C_{2p}}{k}.$$

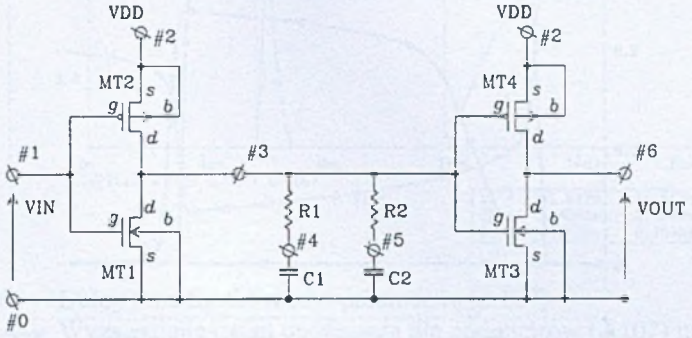


Fig. 2.41. SPICE model of the structure from Fig. 2.39
Rys. 2.41. Model SPICE'a układu przedstawionego na rys. 2.39

The SPICE description of simulated system, has the following form:

```
R1 3 4 28.58K
C1 4 0 0.0994P
R2 3 5 9.48K
C2 5 0 4.333P
VDD 2 0 dc 5
VIN 1 0 PWL(0 0V 5NS 0V 6NS 5V 35NS 5V 36NS 0 45NS 0V)

MT1 3 1 0 0 mdn L=3U W=6U AD=99P AS=99P
+PD=42U PS=42U NRD=1.222 NRS=1.222
MT2 3 1 2 2 mdp L=3U W=6U AD=99P AS=99P
+PD=42U PS=42U NRD=1.222 NRS=1.222
MT3 6 3 0 0 mdn L=3U W=6U AD=99P AS=99P
+PD=42U PS=42U NRD=1.222 NRS=1.222
MT4 6 3 2 2 mdp L=3U W=6U AD=99P AS=99P
+PD=42U PS=42U NRD=1.222 NRS=1.222

.model mdn nmos level=3 vto=0.85 uo=6.1e2 ld=.35u
+tox=640e-10 nsub=8.4e15 gamma=1.9 phi=.686
+eta=1.11 theta=.02 kappa=2.0 mjsw=0.323 rsh=30 js=1.e-12
+vmax=.137e6 xj=.572u cj=3.68e-4 mj=.4 cjsw=5.66e-10
+cgso=.89e-10 cgdo=.89e-10 cgbo=7.5e-10

.model mdp pmos level=3 vto=-0.54 uo=220 ld=.4u
+tox=640e-10 nsub=2.9e15 gamma=.575 phi=.631
+eta=0.2 theta=.14 kappa=6.2 mjsw=0.256 rsh=50 js=1.0e-13
+vmax=0.411e6 xj=0.572u cj=1e-4 mj=0.455 cjsw=2.56e-10
+cgso=.89e-10 cgdo=.89e-10 cgbo=7.5e-10

.tran 3ns 45ns
.print tran v(1) v(3) v(6)
.probe v(1) v(3) v(6)
.end
```

The simulation results for the line parameters (2.107) are presented in Fig. 2.42. For parameters (2.107) we get the transition time for receiver (this is the rise time because we have two inverters) equals 17.3ns and delay time in a system equals 5.6ns. The results in a graphic form are presented in Fig. 2.43 and 2.44.

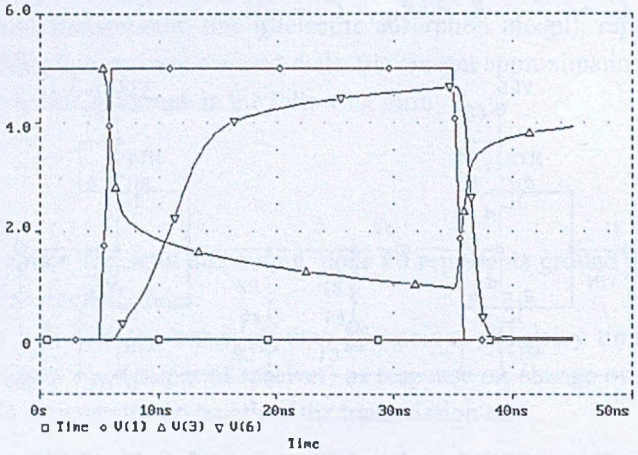


Fig. 2.42. Results of simulation of the structure from Fig. 2.39 for parameters (2.107)
Rys. 2.42. Wyniki symulacji struktury z rys. 2.39 dla parametrów (2.107)

The results of simulation for different k (Eq. 2.108) are collected in Table 2.7.

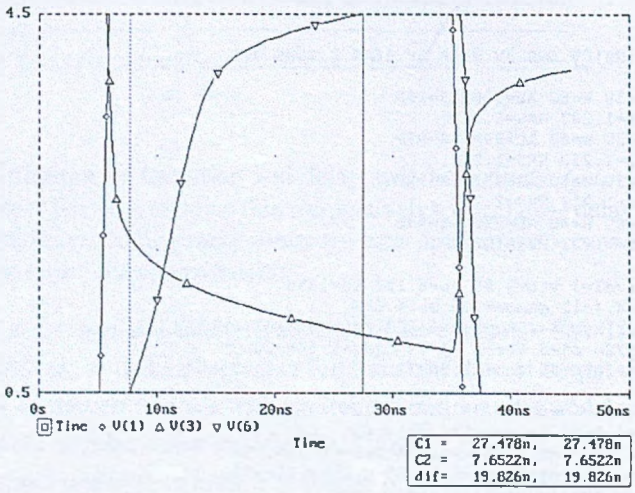


Fig. 2.43. Transition time for the model parameters (2.107)
Rys. 2.43. Wyznaczenie czasu narastania dla parametrów (2.107) modelu

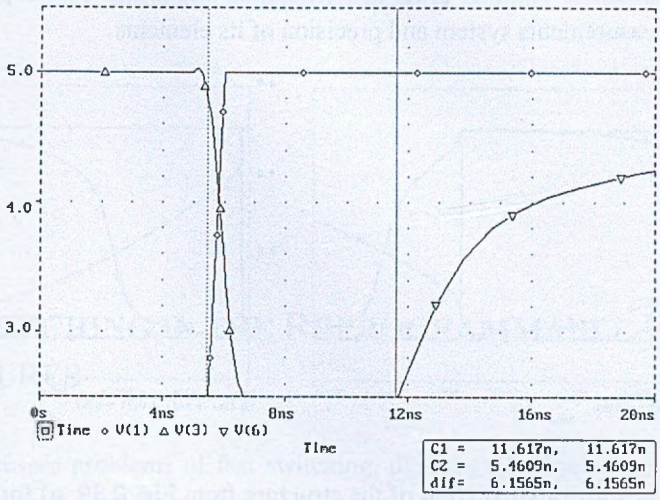


Fig. 2.44. Delay time for the model parameters (2.107)
Rys. 2.44. Wyznaczanie czasu opóźnienia dla parametrów (2.107) modelu

Table 2.7

The transition and delay times of the structure from Fig. 2.39 for transmission line with dielectric losses in dependency on length of the line

k	R_1 [Ω]	C_1 [F]	R_2 [Ω]	C_2 [F]	Transition time [ns]	Delay time [ns]
0.25*	7.145K	0.3976P	2.37K	17.332P	81.71	101.22
0.5*	14.29K	0.1988P	4.74K	8.666P	49.39	37.81
1.0	28.58K	0.0994P	9.48K	4.333P	19.83	6.16
2.0	57.16K	0.0497P	18.96K	2.1665P	3.27	2.45
4.0	114.32K	0.02489P	37.92K	1.08325P	2.26	2.01
8.0	228.64K	12.425F	75.84K	541.625F	2.05	1.88
16.0	457.28K	6.2125F	151.68K	270.8125F	2.02	1.80
32.0	914.56K	3.1063F	303.36K	135.406F	1.98	1.78
64.0	1.829MEG	1.5531F	606.72K	67.703F	1.97	1.77

For longer than 2370μm lines (in Table 2.7 denoted by *), it was necessary an extension of the exiting pulse length until 230ns for completion of measurements in simulation.

Adequate transients (k=0.5 and k=0.25) are presented in Fig. 2.45a and 2.45b respectively.

2.8.7. Concluding Remarks

For theoretical data, the identification algorithm DAMI works properly for high-order approximation (it depends on the computation precision). For experimental data, satisfactory

results can be obtained up to III order approximation and in this case depend on the configuration of the measurements system and precision of its elements.

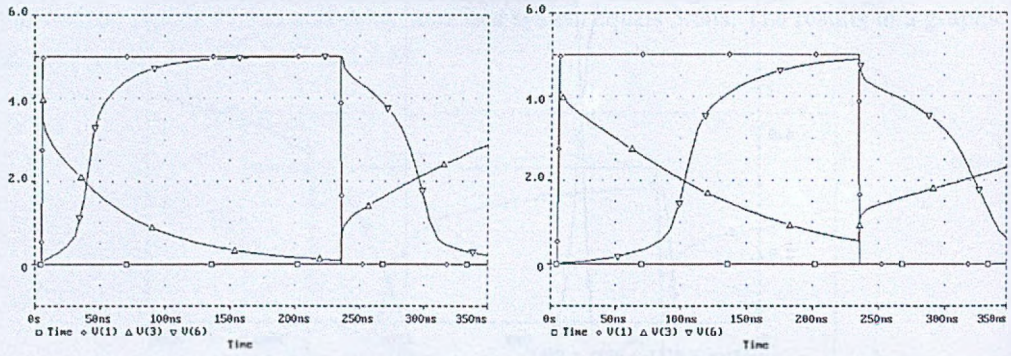


Fig. 2.45. Results of simulation of the structure from Fig. 2.39: a) for $L = 2 \cdot L_p$ (k=0.5), b) for $L = 4 \cdot L_p$ (k=0.25)

Rys. 2.45. Wyniki symulacji struktury z rys. 2.39 dla parametrów: a) $L = 2 \cdot L_p$ (k=0.5), b) $L = 4 \cdot L_p$ (k=0.25)

To improve the accuracy of determination of microstrip line dielectric absorption model in a structure like ST2, one has to use better pulse generator (shorter than 4ns transition time), decrease the value of resistor R_p using the oscilloscope with higher display resolution in mV range, the surface testing probes for the microstrip line and the ground, and printed circuit board specially designed for fixing the testing structure and mounting the elements of the measuring circuit.

Using the real dielectric model parameters in simulation of switching transients for real technological process data, we see the fundamental influence of substrate on the speed of switching. For very short connections (for the given technology determined by the transistors' SPICE models – p. 2.8.6 and geometrical design rules restrictions [Grod93]) less than 70μm (in comparison with the width of inv_min inverter equals to 27μm), for the validated structure and technology, the transition and delay switching times, establish to values 1.97ns and 1.77ns respectively. However, in case of longer interconnections it can be observed strong influence of dielectric absorption in the microstrip lines on degradation of switching characteristics in a VLSI structures of small geometry.

3. Fast Switching in the Reprogrammable FPAA Structures

This chapter discusses problems of fast switching, dynamically reprogrammable mixed-mode systems based on the field programmable analog arrays (FPAA) [Appendix III]. We present circuit solutions based on a modified structure of the CAB (Configurable Analog Blocks) which is an elementary building block in a structure of the FPAA. Modification is performed through external logic control of internal couplings between one or multi-CAB macro blocks. When two or more FPAA cooperate and downloading takes place, a fast switching of the modes of macro blocks can be implemented parallely with selected FPAA download. Thus, the two-layer reconfiguration in the mixed-signal system can be concerned as: a global reconfiguration (download process) which usually is massive but slow, and lower level (partial) reconfiguration (change of mode of selected CAB) inside the FPAA, and which is usually very fast.

Consequently, the switching of the configuration of FPAA can be fulfilled in the two main, hierarchical levels:

global process of changing the configuration of the FPAA called downloading. In this case, the function of the chip is interrupted and the entire structure of the FPAA can be re-loaded. Depending on the method of downloading, a few seconds (approx. 4s through serial communication port of PC computer at 9600 Bauds for MPAA020 chip and 2s for AN10E40 chip) to hundred milliseconds (using EPROM accompanying the FPAA on application board; 100ms for MPAA020, while 30ms for AN10E40 using flash memory) have to be used for global change of structure. This interruption of analog operation is unacceptable in systems operating in continuous time fashion,

the lower level of reconfiguration hierarchy, the attending control logic (ASIC, CLPD or FPGA) changes the functions fulfilled by the FPAA during chip operation. In this case the changes do not involve large number of the CAB, but the changes have to be very fast to stay invisible for application. For recently accessible FPAAs, there is no possibility of switching its parameters values and a part of active structure on-the-fly (during FPAA operation).

The third possibility for the reconfiguration changes is a mixed method using the two above in parallel manner.

In the chapter, the solution of fast switching of the part of working FPAA for adaptive operation is presented (*lower level of reconfiguration*) [Znam98a, PaZn00, PaZn01, ZnPV04]. The solution is based on external control of one or few CABs in the working FPAA.

The solution of "hiding" of the download time and time of transients after download (*global reconfiguration*) is based on parallelization of the FPAAs [ZnPa98a, RZPV99, ZnPR02, Znam98a].

For both solutions: the dynamic (on-the-fly) switching of the CAB cell reconfiguration and switching of FPAAs working in parallel in the systems operating in continuous time fashion, the validation of the solutions and analysis of limitations resulting from hardware imperfections are presented. Finally, the applications of the modified, fast switched FPAAs systems for adaptive and predictive control, and possible application in the microreactors control are presented [ZnPV04, PVZH01].

3.1. Fast Switching of the FPAA Cell

The downloading process of FPAA configuration takes a finite time during which the analog function is interrupted. It is important to note that during this downloading process all cells are placed in a power-down mode i.e. all output signals are set to zero. This feature of FPAA is a serious restriction in continuous-time applications with parameters and/or structure varying. In order to assure proper continuous-time operations from initial time, t_0, to the actual time, t, the system has to be arranged in a parallel connection of two or more FPAA subsystems. In the case of two FPAA's (two subsystems) these components will be called Part1 and Part2 (Fig. 3.1). Analog signals are presented with bold lines. The two parts of the system are alternatively downloaded with the assumption, that part working in analog mode, say Part1 is tracked by newly downloaded part (Part2). Next, when Part1 starts to reload, the tracking Part2 starts to work with proper initial conditions. The time intervals between switching the parts of system may be different (depending on the externally determined need for changing the system parameters), but have to satisfy the condition, that the track mode interval has to precede the time interval of compute mode. The suitable control logic CL for a parallel arrangement of FPAA's can be realized using FPGA technology. Parameters and new structures of this mixed-mode system, can be determined by the control computer and downloaded, in the form of new configurations, to the FPAA chip set in consecutive download phases, of Part1 and Part2 of the system [ZnPa98a].

This method, "hiding" the transient state of downloaded part starting a compute mode, can be improved to shorten the transient state during the switching of MPAA parts, through the use the two-mode operational amplifiers. In general case, the problem can be reduced to implementation of a controlled integrator fulfilling two fundamental modes: tracking the input

signal for proper set of initial condition (*track* mode) and *compute* mode, realized for proper analog function processing.

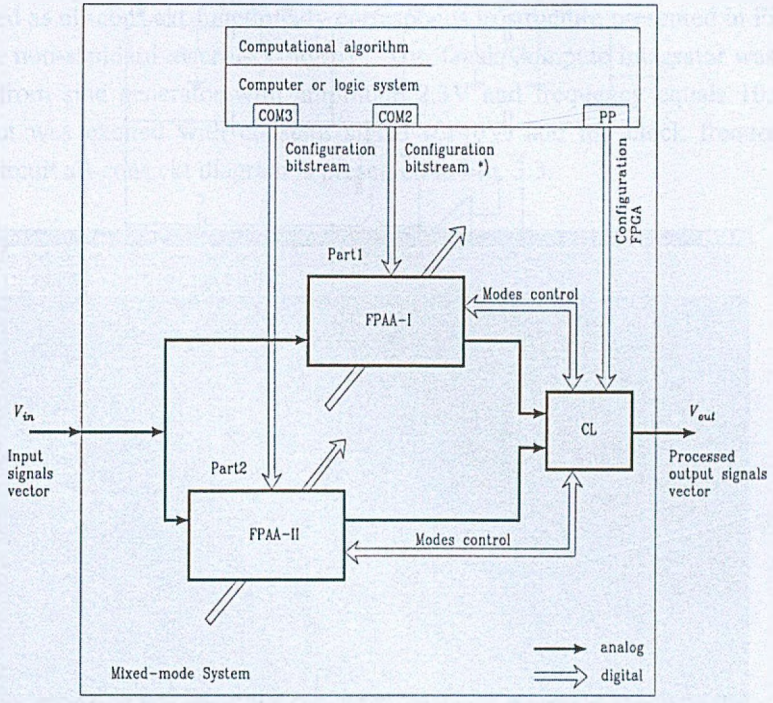


Fig. 3.1. Mixed-mode FPAA system: CL - Control logic (FPGA) and analog multiplexer, *) configuration containing also initial conditions

Rys. 3.1. System mixed-mode zawierający strukturę FPAA: CL – sterujący układ logiczny (FPGA) i multiplekser analogowy, *) konfiguracja zawierająca także warunki początkowe

The initial condition or the track mode of an integrator can be realized using switched unity-gain amplifier controlled by a logic signal [Znam98a, KoKo72]. We shall assume that the integrator is inverting. This structure contains a unity-gain follower W with low impedance switch SW controlled by logic signal R (Fig. 3.2), which is forcing *initial condition* (*track*) mode of the integrator. When the switch SW is ON, the integrating feedback loop is "shunted" to ground via the low output impedance of the unity-gain follower W (and low impedance of the switch SW). The inverter loop stimulated by the tracked voltage (or initial condition voltage) dominates and the integrator is in the *track* (*initial condition*) mode. Dynamics of charging the "integrating" capacitor C is very good because of a low impedance of the loop composed of operational amplifier output, unity-gain follower output, and the switch SW that charges the capacitor C. When the switch SW is OFF, the inverter loop is cut-off and the integrator is in the *compute* mode.

The integrator operation in the two modes can be described using the following relations:

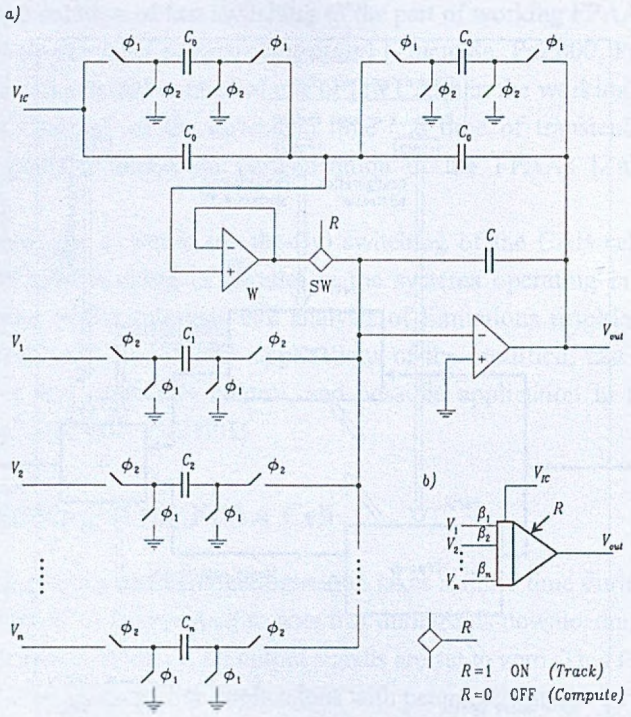


Fig. 3.2. Track/Compute FPAA integrator: a) structure, b) schematic symbol
Rys. 3.2. Sterowany integrator Śledząco/Liczący układu FPAA: a) struktura, b) symbol

Track (*initial conditions*) mode:

$$V_{out}(t_i) = -V_{IC} \tag{3.1}$$

Compute mode:

$$V_{out}(t) = -\sum_{k=1}^{k=n} \int_{t_i}^{t} \beta_k V_k(\tau) d\tau; \qquad V_{out}(t_i) = -V_{IC}\,, \tag{3.2}$$

for i=0,1, 2, ... , where:

$$\beta_k = \frac{C_k f_c}{C}.$$

A symbol f_c describes the clock frequency (for ϕ_1 and ϕ_2 pulses [Moto97a]).

The integrators ought to be capable to work in those two modes for implementation of time-continuous operation of adaptive system (with time varying structure and parameters).

The experiment demonstrating the work of the Track/Compute FPAA integrator was performed for MPAA020 chip and the switch SW (Fig. 3.2) implemented as a one of the chan-

nels of the multiplexer DG408 from Siliconix [Temi97] with forward resistance approximately equal to 80 Ω. The access to the summing point of the operational amplifier was assured through implementation of the two-cell macro "Intgrp1" [Appendix III]. The tested circuit designated as all-cons.ckt functionally corresponds to structure presented in Fig. 3.2, and uses only one non-standard macro – "Intgrp1". The Track/Compute integrator was excited in Track input from sine generator with amplitude 2.3V and frequency equals 10.6kHz. The *compute* input was excited with constant signal 0.140V, and the clock frequency f_c was 1MHz. The circuit all-cons.ckt diagram is presented in Fig. 3.3.

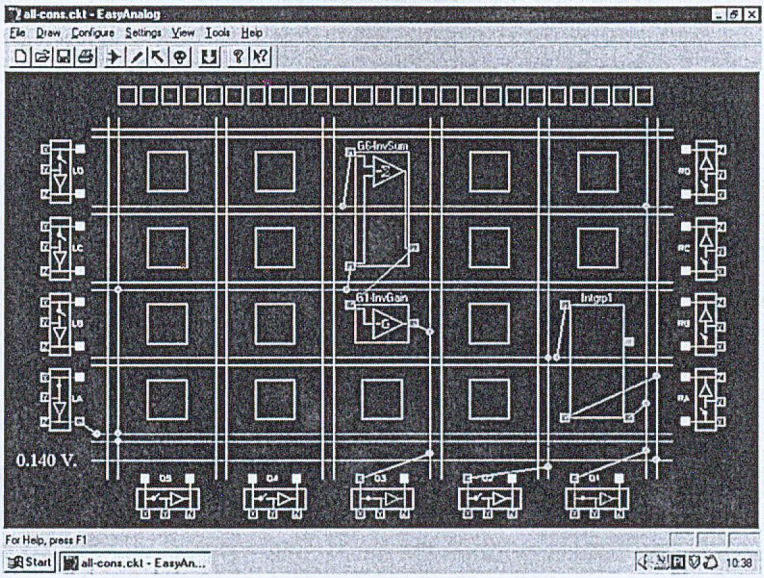


Fig. 3.3. Circuit diagram for Track/Compute integrator excited in *compute* input with constant signal 0.140V

Rys. 3.3. Schemat układu sterowanego integratora Śledząco/Liczącego pobudzanego sygnałem stałym 0.140V

The external controlled switch is connected between pins D3X and D2X, the *initial conditions* input of controlled integrator is LAX pin, the *compute* input is the refence voltage 0.140 V (lowest horizontal wire), and the output of controlled integrator is D1Z pin.

The results of measurements (the output signal for circuit of Fig. 3.3) are presented in Fig. 3.4. The screen of HP54601A downloaded with HP34810B BenchLink Scope program.

Similar discussion can be performed for different modes of operation in the elements of CAB. The idea of controlled operational amplifier in a SC (Switched Capacitors) technique can be generalized. From the accuracy point of view, the one switching element (switching the structure) is the best solution (Eqs. (3.4) and (3.10)). This technique of switching of the structure can be applied not only to the linear SC elements. The feedback elements can per-

form nonlinear operations so the implementation area of reconfigurable structures in FPAA (usually we say about macros) can be extended. The behavioral description of reconfigurable macros e.g. for linear case we can find in the usually used form.

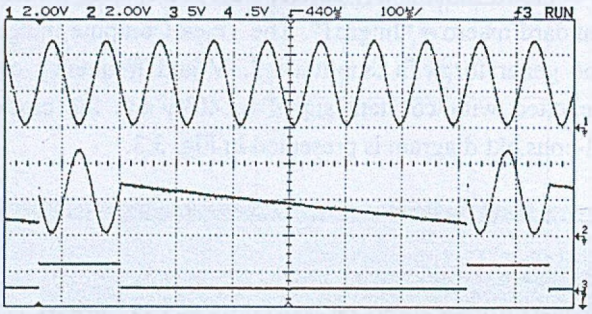


Fig. 3.4. Track/Compute integrator output with constant signal in the *integrating* input
Rys. 3.4. Sygnał na wyjściu integratora Śledząco/Liczącego pobudzanego sygnałem stałym na wejściu *całkującym*

To do this we connect together inputs $V_{IC}(s)$ and $V(s)$ ($V_{IC}(s) = V(s)$) (Fig. 3.5), and for "impedances" $Z_1(s)$, $Z_2(s)$, $Z_3(s)$ and $Z_4(s)$ realized in SC technology, finally we can write:

$$V_{out}(s) = -\left(\frac{Z_2(s)}{Z_1(s)} \times R + \frac{Z_4(s)}{Z_3(s)} \times \overline{R}\right) V(s). \tag{3.3}$$

The symbol × denotes transmittance multiplication by the logic signal R value of 1, or 0. A symbol $\overline{R}$ is used to describe the negation of R. Description of nonlinear operations is more complicated but the switching idea is the same.

3.2. Accuracy Analysis

3.2.1. Track/Compute Integrator Operation

The controlled integrator is presented in Fig. 3.5. The voltage follower (usually designed as a unity-gain) has a very low output impedance R_{wt}.

Logic control signal R switches the switch SW which (in ideal case) has for R=1 the output impedance equals 0Ω, and for R=0 impedance equals infinity. In a circuit the gain of the operational amplifier $k_u \to \infty$, and for working circular frequencies ω there are fulfilled the conditions (in practice R_p is greater than 0Ω):

$$2(R_{wt} + R_p) << R_3, \quad \text{and} \quad 2(R_{wt} + R_p) << \left|\frac{1}{j\omega C}\right|. \tag{3.4}$$

Depending on the logic signal R, the circuit from Fig. 3.5 realizes two operations:

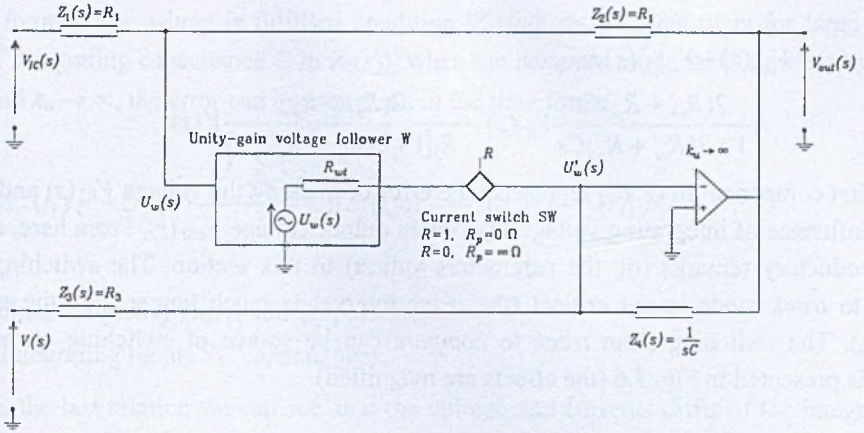


Fig. 3.5. Controlled integrator
Rys. 3.5. Sterowany integrator

When R=1:

$$V_{out}(s) = -\frac{Z_2(s)}{Z_1(s)} V_{IC}(s) = -V_{IC}(s), \tag{3.5}$$

and when R=0:

$$V_{out}(s) = -\frac{Z_4(s)}{Z_3(s)} V(s) = -\frac{1}{sR_3C} V(s). \tag{3.6}$$

The first one is a *track* or *initial conditions* mode, the second is a *compute* mode.

Track* (*Initial Conditions*) *Mode

More precisely, from Fig. 3.5 we can derived the equations of the circuit in *track* mode:

$$\begin{aligned} &\frac{V_{IC}(s)-U_w(s)}{R_1} + \frac{V_{out}(s)-U_w(s)}{R_1} = 0, \\ &\frac{V(s)-U'_w(s)}{R_3} + \frac{U_w(s)-U'_w(s)}{R_{wl}} + \frac{V_{out}(s)-U'_w(s)}{\frac{1}{sC}} = 0, \\ &V_{out} = -k_u U'_w(s). \end{aligned} \tag{3.7}$$

From here, when $k_u \to \infty$ we get:

$$V_{out}(s) = -\frac{1}{1+2(R_{wl}+R_p)Cs} V_{IC}(s) - \frac{2(R_{wl}+R_p)}{R_3[1+2(R_{wl}+R_p)Cs]} V(s). \tag{3.8}$$

In ideal case, the output signal in *track* mode has to have the form:

$$V_{out,id}(s) = -V_{IC}(s), \tag{3.9}$$

so the error in this mode can be expressed by relation:

$$\Delta_T(s) = V_{out}(s) - V_{out,id}(s) =$$
$$= \frac{2(R_{wt} + R_p)Cs}{1 + 2(R_{wt} + R_p)Cs} V_{IC}(s) - \frac{2(R_{wt} + R_p)}{R_3[1 + 2(R_{wt} + R_p)Cs]} V(s). \tag{3.10}$$

The first component in (3.10) represents the error of tracking the voltage $V_{IC}(s)$ and a second, the influence of integrating voltage $V(s)$ on an output voltage $V_{out}(s)$. From here, are derived introductory remarks (on the parameters values) in this section. The switching from *compute* to *track* mode is not critical (the *track* interval is much longer then the time of switching). The switching from *track* to *compute* can be source of switching errors. The situation is presented in Fig. 3.6 (the effects are magnified).

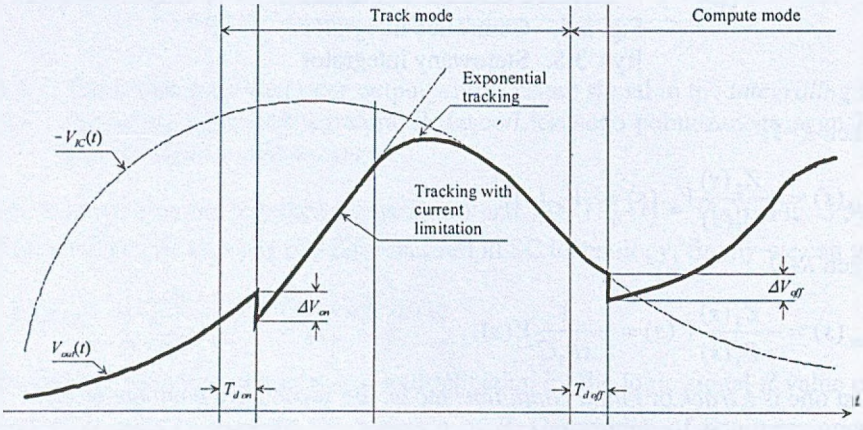


Fig. 3.6. Switching in the Track/Compute integrator
Rys. 3.6. Przełączanie w sterowanym integratorze Śledząco/Liczącym

Delay times $T_{d\,on}$ and $T_{d\,off}$ of the switching have to be minimized, the switching spikes ΔV_{on} and ΔV_{off} can be minimized by the symmetrization of the control part of the switch SW. Tracking with current limitation is caused by real current switch SW. Exponential tracking can be improve with minimizing the time constant $2(R_{wt}+R_p)C$ (3.8). Validation of controlled integrator (including stability conditions) is reported in p. 3.3.1.

Compute Mode

In *compute* mode, the switch SW (Fig. 3.2 and Fig. 3.5) is turned off, so its impedance is very high, but usually to the output of the switch there is the leakage current flowing from node (voltage $U'_w(s)$) via the control and turned off output stage of switch, to the ground. This current is denoted by $i_u(s)$. $U_d(s)$ and $i_d(s)$ are the voltage and current drifts of the operational amplifier at its negative input. Let us assume $Z'_w(s)$ describes impedances of the summing point at the input of operational amplifier to the ground. $Z_3(s)$ is resultant impedance of parallely connected integrating inputs of integrator, and $Z_4(s)$ is a feedback integrating capacitance.

For frequencies, where is fulfilled condition $|Z_4(j\omega)| << |Z'_w(j\omega)|$ (it is for large enough value of integrating capacitance C in $Z_4(s)$), when the *compute* mode takes time interval from 0 to t_1 and $k_u \to \infty$, the error can be expressed in the time form:

$$\Delta_C(t_1) = -U_d(t_1) - \frac{f_c \sum_{k=1}^{n} C_k}{C} \int_0^{t_1} U_d(t)dt + \frac{1}{C} \int_0^{t_1} [i_d(t) + i_u(t)]dt , \tag{3.11}$$

where

f_c - clock frequency (for ϕ_1 and ϕ_2 pulses),

C_k - integrating inputs SC capacitances.

From the last relation we can see, that the voltage and currents drifts of the integrator are critical, because basing on Eq. (3.2) we can rewrite the (3.11) relation in a form:

$$\Delta_C(t_1) = -U_d(t_1) - \sum_{k=1}^{n} \beta_k \int_0^{t_1} U_d(t)dt + \frac{1}{C} \int_0^{t_1} [i_d(t) + i_u(t)]dt , \tag{3.12}$$

where $\sum_{k=1}^{n} \beta_k$ is a sum of the inputs' gains of the integrator.

The possibility to improve the accuracy in *compute* mode when we have to keep unchanged β_k (Eq. (3.2)) is, to decrease drifts, to shorten the computing time t_1 or parallely, increase capacitance C and increase clock frequency f_c (we can also, parallely increase C and C_k for given frequency f_c to keep unchanged β_k, but this decreases rapidly $|Z_3(j\omega)|$ making worse the performance of the controlled integrator). In a case, when the increasing the value of the capacitance C is applied, it is necessary to decrease considerably the value of the R_p+R_{wt} resistance, to save the quality of the work of the controlled integrator in a *track* mode. The last changes (increasing the capacitance C) are limited with the large value of the current flowing through the output stage of the operational amplifier in Compute mode, and operational amplifier, follower W, and switch SW in *track* mode. Comparing the equations (3.12) and (3.2) we see, that the additional way to improve accuracy in *compute* mode, is to fulfill the condition:

$$|V_k(j\omega)| >> |U_d(j\omega)|,$$

i.e. it is necessary the proper scaling of the variables $V_k(s)$ in a system.

3.3. Validation of the Switched Cell Structures

3.3.1. Controlled Integrator

The experiments were performed for MPAA020 chip and the switch SW (Fig. 3.2) implemented as the structure in Fig. 3.3, however in this case, the *compute* input was excited

with the same sinusoid as the *track* input (amplitude 2.3V, frequency 10.6kHz). The circuit diagram is presented in Fig. 3.7.

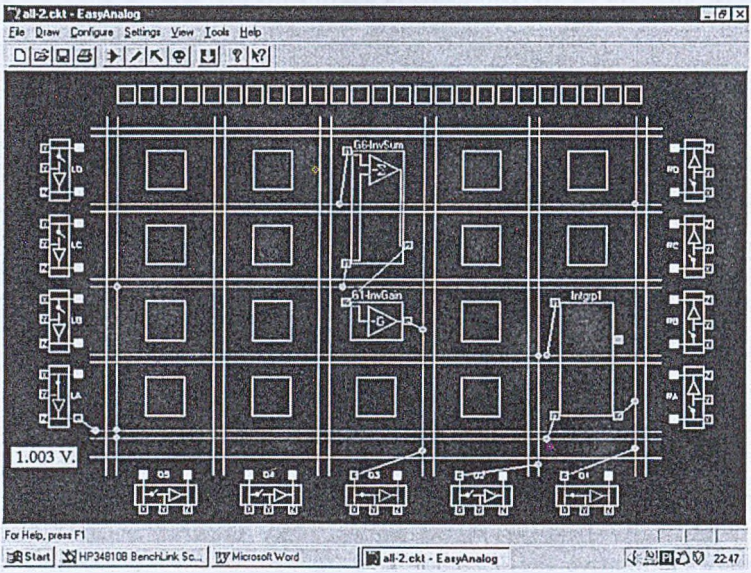


Fig. 3.7. Circuit diagram for Track-Compute integrator excited in *track* and *compute* inputs from external sine generator, and controlled through external switch (signal R – Fig. 3.2)

Rys. 3.7. Układ integratora Śledząco/Liczącego sterowanego zewnętrznym kluczem (sygnał R – rys 3.2), pobudzanego na wejściach *śledzącym* i *całkującym* sygnałem sinusoidalnym

The results of measurements for different time of *track* modes are presented in Figs. 3.8 and 3.9 (The screens of HP54601A downloaded with HP34810B BenchLink Scope program).

The measurement results presented in Fig. 3.9a are obtained for shorter *track* time interval than in Fig. 3.8.

The details of Fig. 3.9a in the transition of the integrator's output from *compute* to the *track* mode with transient state equal approximately 3μs, are shown in Fig. 3.9b.

The circuit diagram for inspection of the transition at the output of integrator from *track* to *compute* mode, for constant signal at the integrating input (0.140V) and identical signals and parameters as earlier, was presented in Fig. 3.3, and the output signal in Fig. 3.4. The details of transient state interval from *track* mode to the *compute* mode are presented in Figs. 3.10a and 3.10b for increasing time base of diagrams.

Fig. 3.9b shows that the transient time in *compute* to *track* state needs approx. 3μs and in the case of transition from *track* to *compute* state it is 600ns with amplitude error of the level of 100mV (Fig. 3.10b).

Experimentally found stability conditions for controlled FPAA integrator are following:

1. For $R_p \approx 100\Omega$, $a=0.3$,
2. for $R_p=0\Omega$, $a=0.66$,

where:

R_p – the resistance of the switch SW (Fig. A.1),
a – the gain of the voltage follower W.

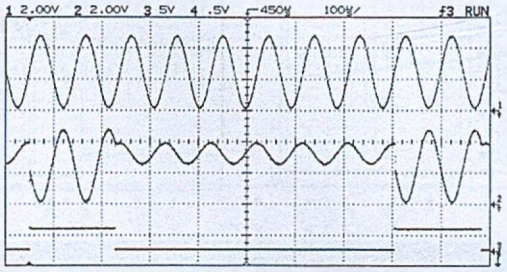
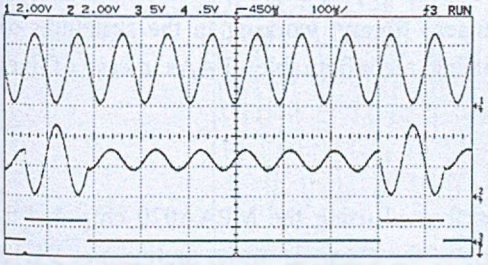


Fig. 3.8. Measurements results in Track-Compute integrator. Channel 1 represents sine signal at the *track* input and *compute* input of integrator, channel 2 represents output of integrator, and channel 3 is control signal R (Fig. 3.2) equals High for *track* mode and Low for *compute* mode

Rys. 3.8. Wyniki pomiarów integratora Śledząco/Liczącego. Kanał 1 – sygnał sinusoidalny na wejściach *śledzącym* i *całkującym*, kanał 2 – sygnał wyjściowy integratora, kanał 3 – sygnał sterujący R (rys. 3.2, H dla stanu *śledzenia*, L dla *całkowania*)

a)



b)

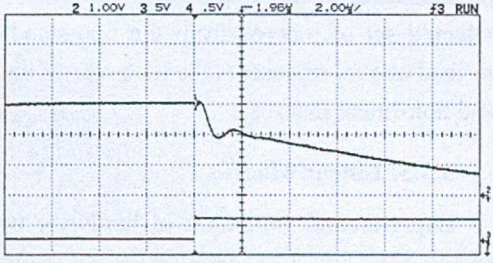


Fig. 3.9. Track/Compute integrator: a) shorter time of *track* mode, different value of initial condition for integrating input, b) details in transition of output of integrator from *compute* to *track* mode

Rys. 3.9. Sterowany integrator Śledząco/Liczący: a) krótszy czas trwania stanu *śledzenia*, inna wartość warunku początkowego, b) szczegóły stanu przejściowego na wyjściu integratora ze stanu *liczenia* do stanu *śledzenia*

The measurements indicate that the new technique with external control of the selected cell significantly improved the FPAA switching conditions, e.g. in the case when the "hiding" of transients state takes place (this is a very fast configuration switching) we need approximately 600μs, while in the presented method this requires not more than 3μs. Moreover, this

technique can be extended to the general area of reconfigurable FPAA systems. This can be applied for implementation of continuous-time reconfigurable dynamic mixed-mode systems.

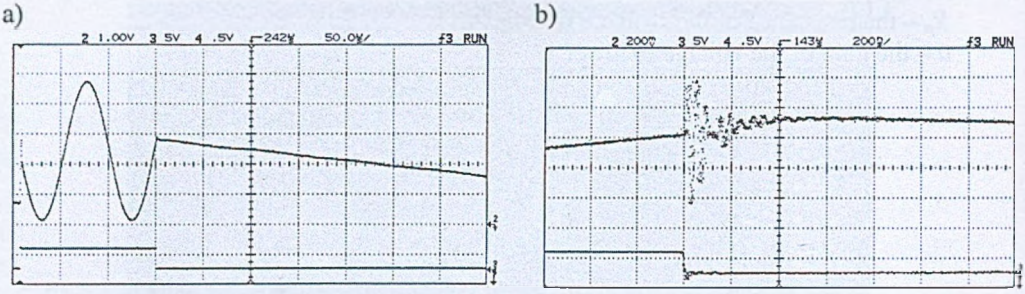


Fig. 3.10. Track/Compute integrator: a) details of *track* to *compute* transition structure, b) details of transition state from Fig. 3.10a

Rys. 3.10. Sterowany integrator Śledząco/Liczący: a) szczegóły stanu przejściowego ze stanu *śledzenia* do stanu *liczenia*, b) szczegóły stanu przejściowego z rys. 3.10a

3.3.2. Reconfiguration of Macros

Reconfiguration in lower layer of hierarchy of reprogrammable FPAA presented in the work is based on one-switch, and the on-the-fly changes of the operational amplifier feedback. The access to the summing point of the operational amplifier was assured through implementation of the single-cell or multi-cell structures in properly constructed macros. The selected set of macros from the non-standard macro library, working in the structures described above, represents the behavior of the switched reconfigurable FPAAs in case of linear and non-linear macros.

3.3.3. Linear Macros

Experimental validation of hardware was performed using the MPAA020 chip and the switch SW (Fig. 3.5) implemented exploiting one of the channels of the multiplexer DG408 [Temi97, Maxi01] with forward resistance approximately equal to 80 Ω.

The two-amplifiers circuit with different gain (–1 and –2) in a reconfigurable structure (switching macro structure) is presented in Fig. 3.11 (the circuit designated as M-UGA.ckt).

The macros MM3 (Gain –2), RES (Gain –1), and UGA (Gain +1) are constructed as a one-cell (CAB) or two-cell SC structures. The MM3 macro contains the main operational amplifier in the circuit. The input line of the buffers D3X and D2X are connected to the external digitally controlled analog switch. The circuit is excited from sine-wave generator with amplitude 2V peak-to-peak and frequency 15kHz (LAX buffer of the FPAA chip). The proper inputs of macros MM3 and RES are excited using this same signal. The clock frequency f_c was 1MHz, and the ratio for the capacitors C_1/C_3 (C1-1/C-1, see Fig. 6.8) inside of macro MM3 was 10/5 and for capacitors C_1/C_3 inside of macro RES was 10/10.

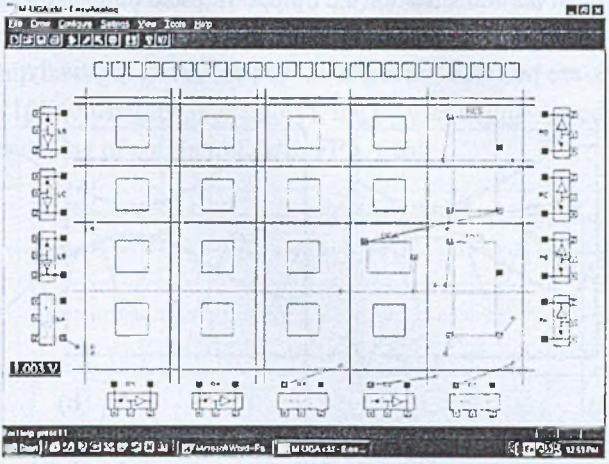


Fig. 3.11. Circuit diagram for two-macro excited from external sine generator, and controlled through external switch (controlled through signal R – Fig. 3.5)

Rys. 3.11. Układ dwu makr sterowanych zewnętrznym kluczem (sterowanym sygnałem R – rys. 3.5) pobudzanym z zewnętrznego generatora sinusoidalnego

The results of measurements for transient states of switched circuit M-UGA at output with reference to control signal at the input of external switch are presented in Figs. 3.12 and 3.13.

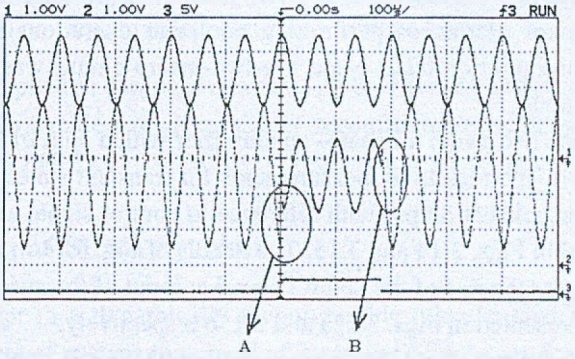
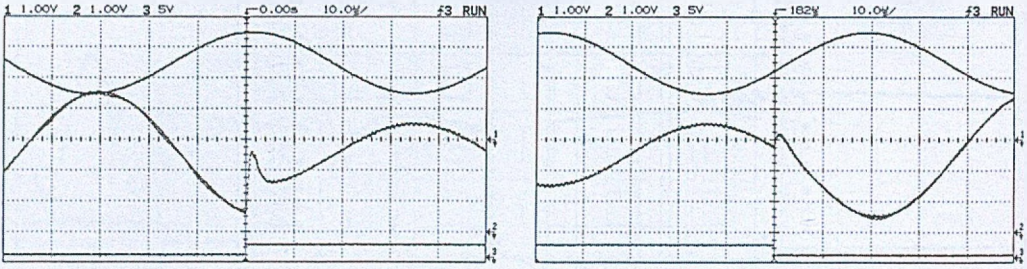


Fig. 3.12. Measurements results in linear macros switched via external logic controlled switch (channel 2). Channel 1 represents sine-wave signal at the analog input of the circuit, and channel 3 is a control signal R (Fig. 3.5) at the digital input of the external switch

Rys. 3.12. Wyniki pomiarów przełączania dwu liniowych makr przez zewnętrzny klucz sterowany sygnałem logicznym (kanał 2). Kanał 1 – sygnał sinusoidalny na wejściu analogowym układu, kanał 3 – sygnał sterujący R (rys. 3.5) na wejściu cyfrowym zewnętrznego klucza

The screens of HP54601A scope were downloaded with HP34810B BenchLink Scope program through the HP54650A HP-IB Interface Module and HP82341D Card HP-IB for PC.

The details of Fig. 3.12 in the transition of the output of tested circuit, for the rise of the control signal at the switch (channel 3) designated in Fig. 3.12 as a A area, and for a fall of the control signal (B area), are presented in Figs. 3.13a and 3.13b respectively.



a) b)

Fig. 3.13. Details in transition of output of the linear two-macro circuit: a) rise of the control signal (Fig. 3.12, A area), b) fall of the control signal (Fig. 3.12, B area)

Rys. 3.13. Szczegóły stanu przejściowego na wyjściu układu zbudowanego na dwu liniowych makrach: a) zbocze narastające sygnału sterującego (rys. 3.12, obszar A), b) zbocze opadające sygnału sterującego (rys. 3.12, obszar B)

Figs. 3.13a and 3.13b show that the transient time in the reconfigurable CAB implementing linear macros is not longer than 5µs.

3.3.4. Nonlinear Macros

To check the behavior of macros performing nonlinear operations and to verify their function when the reconfiguration takes place, the two-macro circuit was tested in the same conditions as a linear circuit.

The tested circuit has two parts: a linear – an amplifier with a gain of –2, and a full-wave rectifier with gain of +1. The results of measurements for transient states of switched circuit (designated as Amp-Frect.ckt) at output with reference to control signal at the input of external switch are presented in Figs. 3.14 and 3.15. The details of Fig. 3.14 in the transition of the output of tested circuit, for the rise of the control signal at input of the switch, and for a fall of the control signal, are presented in Figs. 3.15a and 3.15b respectively.

Fig. 3.15 shows that the transient time in the reconfigurable CAB implementing nonlinear macros is not longer than 8µs.

3.3.5. Concluding Remarks

The measurements indicate that the new technique of switching of the CAB cell's mode in the selected cells, dramatically improved the dynamics of switching in the reconfiguration process of the FPAA chip. In case of single controlled amplifier (Track/Compute integrator) the transient time of switching is approx. 3µs, in switching of the linear macro structure requires not more than 5µs, and for non-linear macros approx. 8µs conditions. In comparison with other methods of reconfiguration like the "hiding" of transients state in multi-chip FPAA

system (we need approximately 600μs – see p. 3.5) or the FPAA downloading (from approx. 4s through serial communication port of PC computer at 9600 Bauds for MPAA020 chip and 2s for AN10E40 chip through 100ms for MPAA020 using EPROM accompanying the FPAA, while 30ms for AN10E40 using flash memory), the new technique speeds up over three order of magnitude the switching of configuration in FPAA chip.

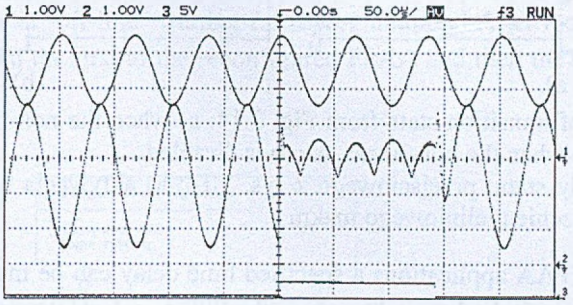


Fig. 3.14. Measurements results in non-linear macro switching via external logic controlled switch (channel 2 - middle). Channel 1 – upper, represents sine-wave at the analog input of circuit, and channel 3 – lower, is a control signal *R* (Fig. 3.5) at the digital input of the external switch

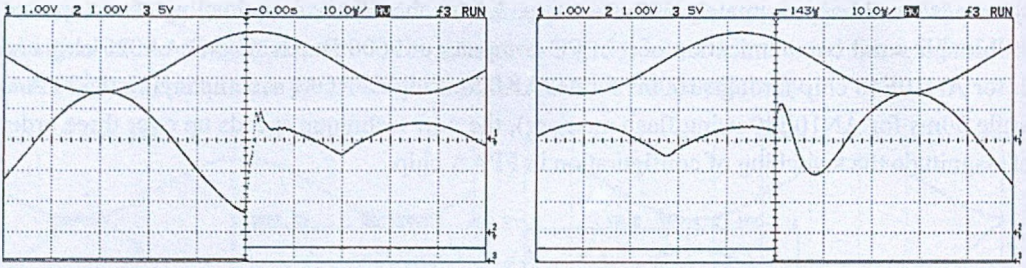
Rys. 3.14. Wyniki pomiarów przełączania nieliniowego makra przez zewnętrzny klucz sterowany sygnałem logicznym (kanał 2 – środkowy). Kanał 1 – górny, sygnał sinusoidalny na wejściu analogowym układu, kanał 3 – dolny, sygnał sterujący *R* (rys. 3.5) na wejściu cyfrowym zewnętrznego klucza

This technique applied in conjunction with a global reconfiguration (downloading), allows very effective implementation of dynamically reconfigurable continuous-time mixed-mode systems [ZnPV04, PVZH01].

3.4. Switching of FPAA Systems

The basic concept in a dynamically reconfigurable mixed-signal hardware is presented here using an example of system composed of 2 parallel FPAAs, analog multiplexer and multiplexer's control logic (addressing FPAA and switching time delay settings). In the reported experiments all the control was determined using a PC and the software EasyAnalog (or AnadigmDesigner) [Appendix III]. The experimental setup was primary intended for investigations of switching inaccuracies and performance imperfections caused by the hardware.

A more sophisticated control system, implemented on FPGA, can be used to analyze the input signal and generate the desired transfer function in a reprogrammable modes. FPGA provides a time delay for the switching, which is necessary to minimize the effect of perturbations that are investigated in this work. A very rapid reconfigurable system can be constructed using several FPAAs that are being reconfigured and switched by FPGA.



a) b)

Fig. 3.15. Details of transition state from Fig. 3.14: a) when the non-linear macro is activated, b) when the non-linear macro is disabled

Rys. 3.15. Szczegóły stanu przejściowego z rys. 3.14: a) aktywacja nieliniowego makra, b) wyłączenie nieliniowego makra

For each of the FPAA applications a specified time delay can be modeled and applied to the system in the form of a look-up table where the FPGA, selects the appropriate time delay. The block diagram of such a system is shown in Fig. 3.16.

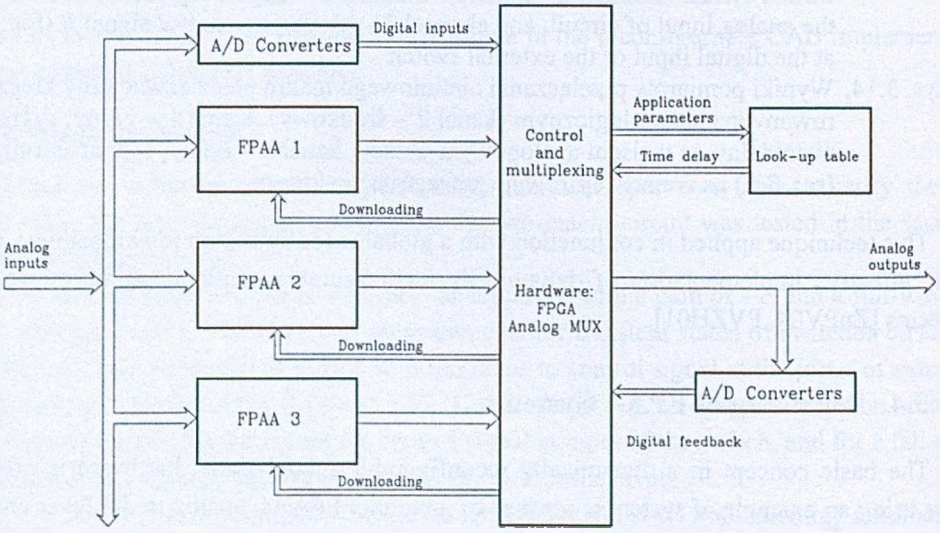


Fig. 3.16. Block diagram of the dynamically reconfigurable system using a FPGA with a look-up table and blocks of analog programmable chips (FPAA)

Rys. 3.16. Schemat blokowy systemu mixed-mode rekonfigurowanego dynamicznie, wykorzystującego układ FPGA z pamięcią (tablica parametrów) oraz reprogramowalne układy FPAA

3.4.1. Dynamically Reconfigurable Two FPAAs Adaptive System

The block diagram of the dynamically reconfigurable two FPAAs system is shown in Fig. 3.17. A control signal for the multiplexer [Temi97] is generated on the FPAA output. When

the FPAA starts to work after reconfiguration, a 'HIGH'- signal appears at an output pin that enters into an adjustable time delay circuit on the control board and then to the multiplexer to interchange the analog outputs of the FPAAs. The time delay circuit is established in order to introduce a time lag between the end of the reconfiguration phase, when the reprogrammed FPAA starts processing the input signal, and the physical switching of the multiplexer to the output of the reconfigured FPAA. In this system one FPAA can filter the analog input signal while the second one is "off-line" waiting for reprogramming. After reconfiguration the multiplexer switches from the first to the reconfigured FPAA and then the other one is ready for reprogramming.

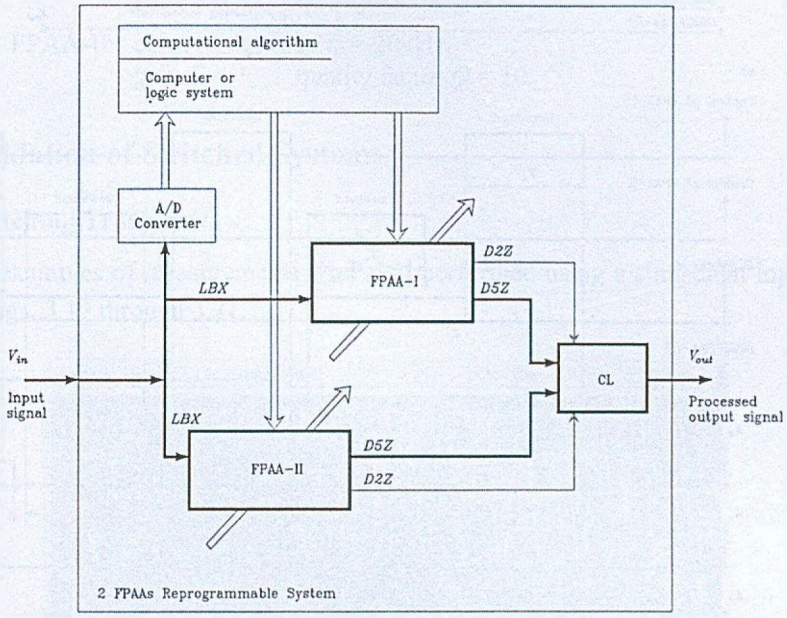


Fig. 3.17. Block diagram of the dynamically reconfigurable two FPAAs adaptive system: CL - Control logic and analog multiplexer, *D5Z* - processed analog signal, *D2Z* - digital control signal to CL

Rys. 3.17. Adaptacyjny system dwu dynamicznie rekonfigurowalnych układów FPAA: CL – sterujący układ logiczny z multiplekserem analogowym, *D5Z* – przetwarzany sygnał analogowy, *D2Z* – wejściowy, sterujący sygnał logiczny układu CL

The system using two FPAAs provides a steady output signal without an interruption when redefinition of the analog filter function is needed, such as changing the quality factor or adjusting the corner frequency [ZnPa98a].

The described process is illustrated in the timing diagram in Fig. 3.18. A complicating factor of the dynamic reconfiguration is the transition behavior of the switching from one FPAA to the other. After the FPAA is reprogrammed it cannot be put immediately "on-line" because the signal needs some time to settle and reach a steady state. That's why it is neces-

sary to provide a time delay (T_S) between the end of the programming phase (T_p) and the actual physical switching.

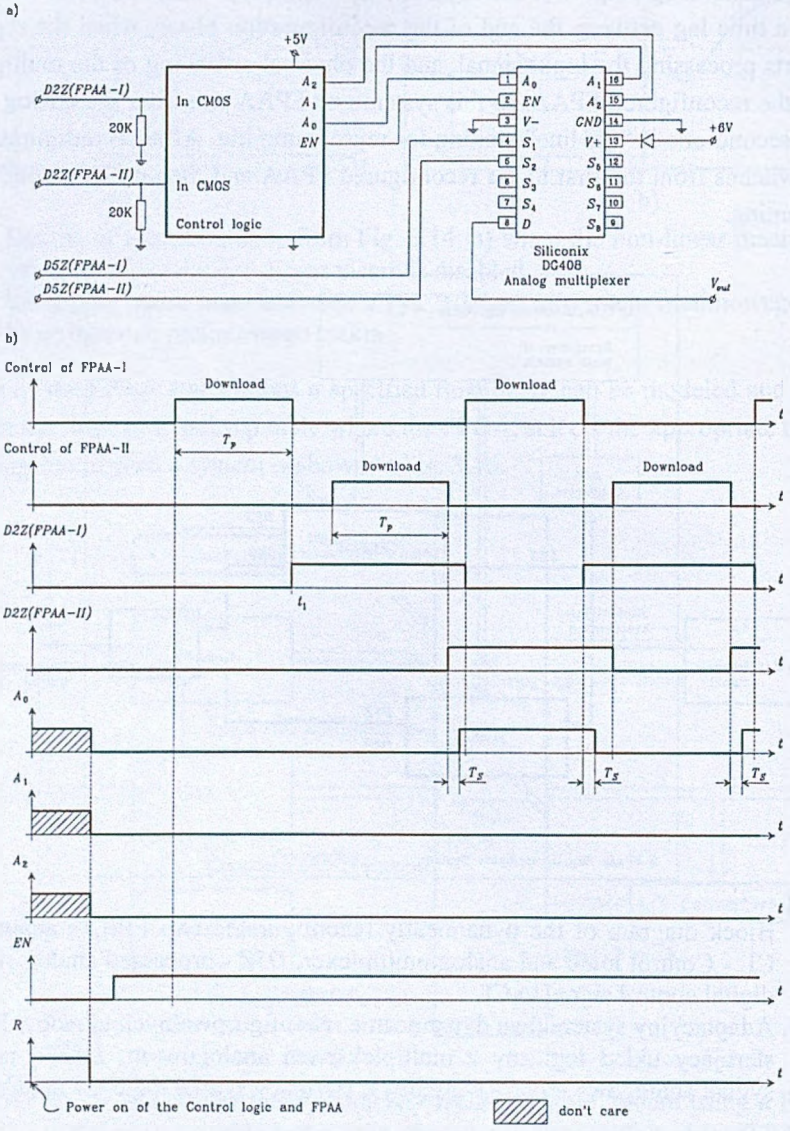


Fig. 3.18. Timing of reprogramming and filtering of 2 parallel FPAAs for uninterrupted processing of an analog input signal: a) CL circuit diagram (Fig. 3.17), b) Timing (R - the Control logic internal, initializing signal)

Rys. 3.18. Czasowa sekwencja sterująca reprogramowaniem i filtracją w układzie dwu równoległych układów FPAA przetwarzających sygnał analogowy w sposób ciągły: a) CL schemat blokowy układu (rys. 3.17), b) czasowa sekwencja sterująca (R – wewnętrzny sygnał sterujący inicjalizacji)

During programming of a FPAA the chip is reset and all capacitors are discharged. The output is also set to earth ground in contrast to the signal ground of 2.5V established on the chip during processing. Considering the 'jump' of 2.5V from earth to signal ground the transition behavior can be modeled as a step response of a system of second order with typical exponential settling behavior of a FPAA biquad.

The circuit has been analyzed using sinusoidal analog input signals with small amplitudes as typically used in data processing applications.

The following parameters of the filters (macro F6 [Moto97b]) were assumed:

FPAA-I: corner frequency $f_0 = 20$kHz,
gain $G = 1$, quality factor $Q = 4$,

FPAA-II: corner frequency $f_0 = 20$kHz,
gain $G = 1$, quality factor $Q = 10$.

3.5. Validation of Switched Systems

3.5.1. Switching Transients

A typical examples of measurements [HePa96] performed using a sinusoidal input signal are given in Figs. 3.19 through 3.21.

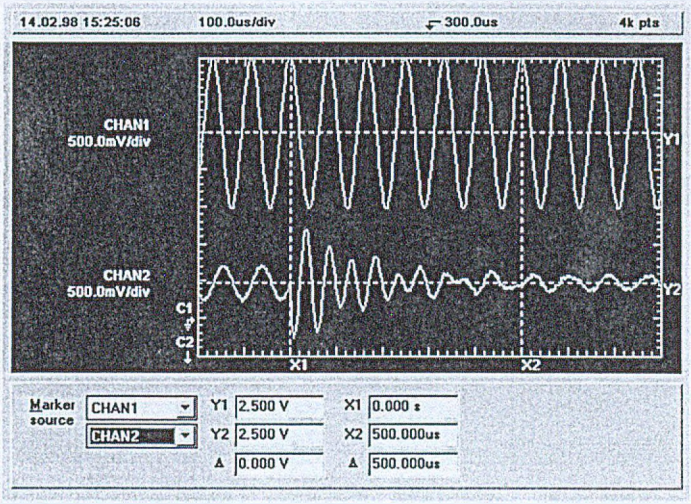


Fig. 3.19. Transients in the filter after downloading, illustrating the need for additional delay before multiplexing (switching for analog signal frequency f=12kHz)

Rys. 3.19. Stan nieustalony w filtrze FPAA po zakończeniu wpisu konfiguracji, ilustrujący potrzebę wprowadzenia dodatkowych opóźnień w trakcie multipleksowania kanałów (przełączenie przy częstotliwości sygnału analogowego f=12kHz)

The time interval T_S was 1.9μs and a clock frequency of the FPAAs was 1MHz. The frequency of the sinusoidal input signal at the input of the system was 12kHz, 20kHz, and 40kHz

respectively. The extension of the T_S from 1.9μs over 500μs allows to "hide" the transient state of the activated FPAA. The output signal of the reconfigurable system for delay T_S = 589.9μs is shown in Fig. 3.22. In this case, the frequency of the sinusoidal input at the input of the adaptive filter (Fig. 3.17) was 18kHz.

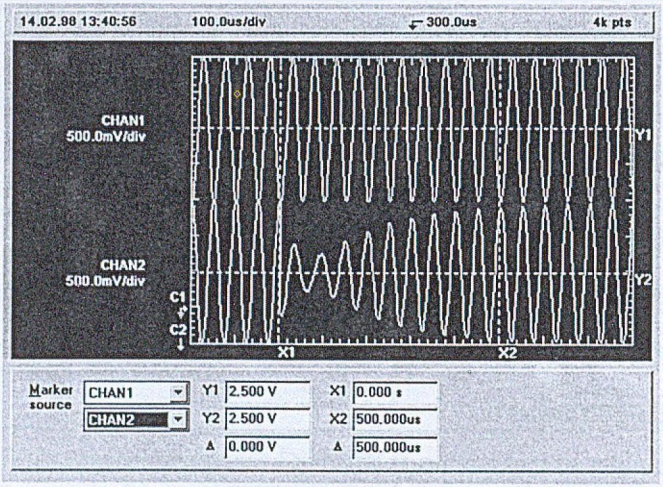


Fig. 3.20. Filter switching (f = 20kHz)
Rys. 3.20. Przełączanie filtra dla częstotliwości f = 20kHz

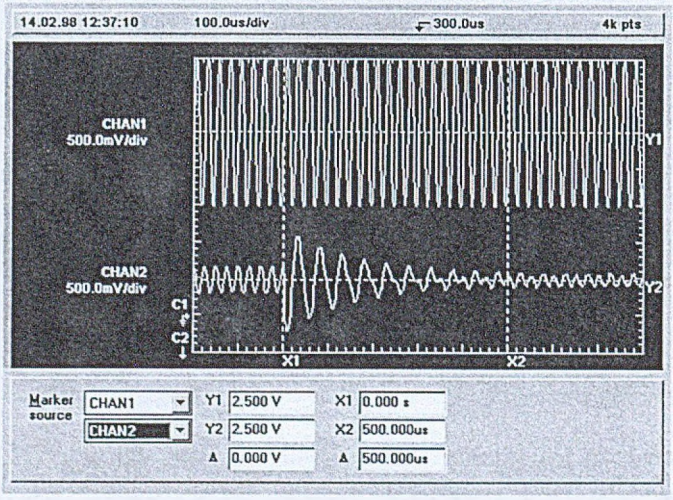


Fig. 3.21. Filter switching (f = 40kHz)
Rys. 3.21. Przełączanie filtra dla częstotliwości f = 40kHz

During various measurements it was observed that for both inputs, step function and sinusoidal signal, the output is forced into the same exponential envelope.

This means that the measured settling time of a step input is also the time period within which the sinusoidal signal settles in. Thus, a constant step function as the input signal was utilized during the measurements of the settling time.

Time Response of Systems of 2nd Order

The modeling for the settling time presented here is applicable to any second-order system (biquad). The transfer function of a band pass biquad filter is

$$H(s) = -\frac{2\pi f_0 \frac{G}{Q} \cdot s}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2}, \tag{3.13}$$

where G is the pass-band gain, Q is the quality factor, and f_0 is the corner frequency of the filter. The time response of this system is characterized by the roots of the denominator polynomial $q(s)$, which in fact are the poles of the transfer function. The denominator polynomial $q(s)$ is therefore called the characteristic polynomial and

$$q(s) = 0, \tag{3.14}$$

is the characteristic equation.

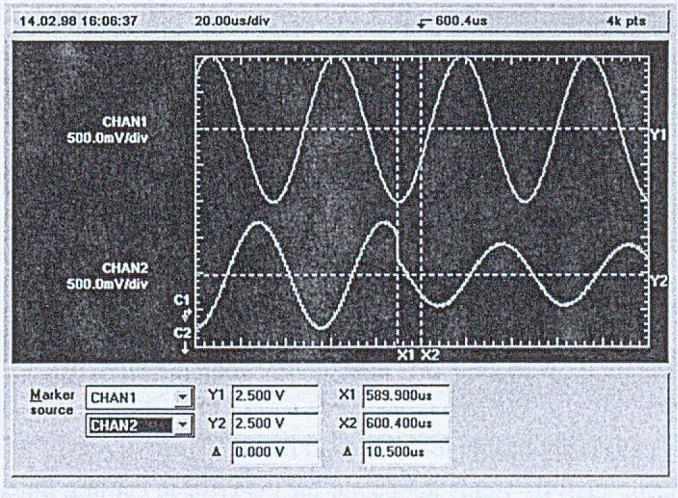


Fig. 3.22. Result of switching/multiplexing with the delay assuring steady state in the reprogrammed filter

Rys. 3.22. Wynik przełączania i multipleksowania z opóźnieniem zapewniającym stan ustalony na wyjściu reprogramowalnego filtra

The characteristic equation of the system under consideration is

$$s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2 = 0. \tag{3.15}$$

For the unit-step input the Laplace inversion of the proper transfer function yields the output time response [NaGo75] given by

$$h(t) = -\frac{\frac{G}{Q} e^{-\frac{\pi f_0}{Q} t}}{\sqrt{1-\frac{1}{4Q^2}}} \sin\left(2\pi f_0 \sqrt{1-\frac{1}{4Q^2}} \cdot t\right). \tag{3.16}$$

The steady-state $h(t)$ is given in a form

$$h_{SS} = \lim_{t\to\infty} h(t) = 0. \tag{3.17}$$

It can be observed that for Q>0.5 the time response $h(t)$ oscillates between a pair of envelopes before reaching steady-state. The transient is comprised of a product of an exponentially decaying term $e^{-\frac{\pi f_0}{Q}}$ and a sinusoidally oscillating term $\sin\left(2\pi f_0 \sqrt{1-\frac{1}{4Q^2}} \cdot t\right)$.

The time constant of the exponential envelope is $T = \frac{Q}{\pi f_0}$. The settling time t_s is defined as the time period the signal needs to get within a certain tolerance band around the steady-state value and stays within these bounds. Considering only the exponentially decaying envelope for a tolerance band of 1% the settling time is given by

$$\frac{e^{-\frac{\pi f_0}{Q} t_s}}{\sqrt{1-\frac{1}{4Q^2}}} = 0.01. \tag{3.18}$$

For Q>>0.5 we have $e^{-\frac{\pi f_0}{Q} t_s} \approx 0.01$. This yields the settling time t_s

$$t_s = \frac{4.605Q}{\pi f_0}. \tag{3.19}$$

The equation (3.19) is applicable for all biquad filters.

A first order error analysis yields the bound for the error in settling time, Δt_s, as a function of error bounds on quality factor, ΔQ, and corner frequency, Δf_0, in the form:

$$|\Delta t_s| \le \frac{4.605}{\pi f_0} \cdot |\Delta Q| + \frac{4.605Q}{\pi f_0^2} \cdot |\Delta f_0|. \tag{3.20}$$

The quality factor, Q, given in [Anad01d] is determined by the formula:

$$Q = \frac{C_A}{C_4}. \tag{3.21}$$

The analysis of errors in MPAA020 implementation of filter, which is mainly caused by capacitor imperfections [PGAA98, Anad01d], yields:

$$|\Delta Q| \le \frac{1}{C_4} \cdot |\Delta C_A| + \frac{C_A}{C_4^2} \cdot |\Delta C_4|. \tag{3.22}$$

The capacitor C_A is kept at its maximum and to increase the Q it is necessary to decrease C_4. The decrease in C_4 causes an increase of its error, ΔC_4, and an increase in the error bound of Q. The bound on errors in frequency f_0 is not affected by the changes in the quality factor Q. Consequently on increase in Q, causes on increase of error bound on settling time, which was indeed observed in our measurements (Fig. 3.23) as higher fluctuations in the settling time occurring at higher values of Q.

3.5.2. Measurements of Settling Time

The measurements were performed to verify the modeling of the settling time and to demonstrate that the described settling time model is applicable for both an input step function and sinusoidal signals. A constant pass-band gain of G=1 was used in all measurements.

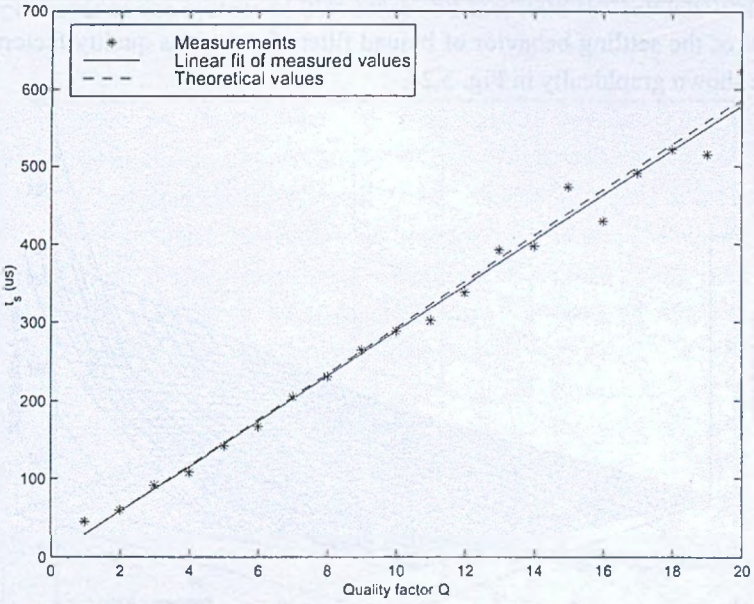


Fig. 3.23. Settling behavior of band pass filter at corner frequency of 50kHz
Rys. 3.23. Czas ustalania w filtrze środkowo-przepustowym dla częstotliwości centralnej 50kHz

The low resolution of the oscilloscope made it difficult to get the exact time when the signal deviation is smaller than 1%. Especially for low settling time values in the high frequency range and for quality factors smaller than the value of one it is very difficult to obtain mean-

ingful results, therefore there are only results of measurements with high Q ($1<Q<20$) filters presented. Additionally, the measured points were not situated exactly on a "straight line". In order to get a more meaningful analysis of the measured values, the measurements were approximated using a straight line determined by the method of linear regression [Weis85].

Cumulative results of measurements of the settling time as a function of the biquad quality factor are shown in Fig. 3.23. The plot shows that indeed the behavior of a band pass biquad filter (high Q) with corner frequency of 50kHz follows the analysis presented here.

The relative error between the calculated and the linear fit of this measured values is 1.48% and is mainly caused by reading errors of the oscilloscope due to the low resolution. The errors of other filter measurements are shown in Table 3.1.

Table 3.1

Relative errors of the measured settling time of various filters

Filter	band pass	high pass	high pass	band stop	low pass
Corner frequency	10kHz	25kHz	100kHz	50kHz	25kHz
Relative error	3.24%	2.05%	0.55%	1.33%	4.51%

The model of the settling behavior of biquad filters for various quality factors and corner frequencies is shown graphically in Fig. 3.24.

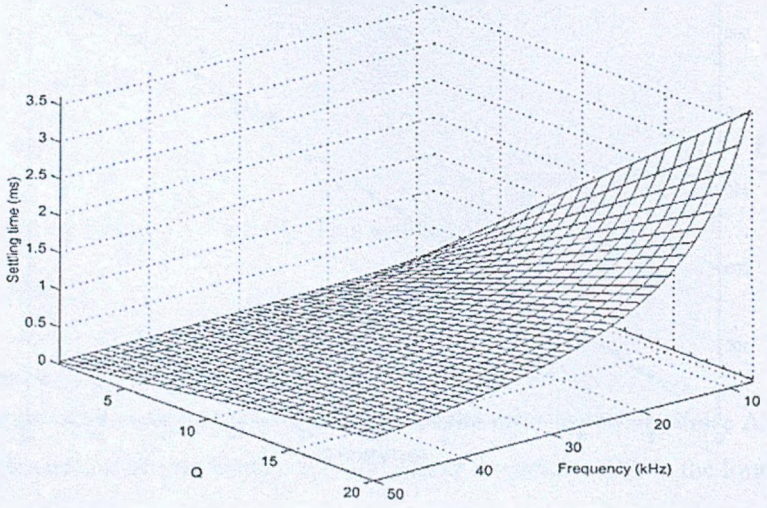


Fig. 3.24. Settling time behavior versus quality factor and corner frequency
Rys. 3.24. Czas ustalania w funkcji dobroci i częstotliwości centralnej

This graph indicates that the settling time increases significantly with increasing quality factor, especially for very low corner frequencies. Therefore, the time delay for the switching of the output of the reconfigured FPAA has to be adjusted appropriately in order to avoid

perturbations. This time delay must be indeed particularly long for the filters implemented with a low corner frequency and a high quality factor.

Cascading Biquads

In practice, filters of higher order are commonly used because their performance, such as for example the transition band, can be improved by a system of higher order. A filter of higher order is obtained cascading blocks of filters of first or second order. With the 20 analog cells of the FPAA it is possible to realize a filter of 20^{th} order on one FPAA.

It is also necessary to investigate the settling behavior of these filters to develop a model for the prediction of the time delay that is needed for the reconfiguration process. In a simple experiment we measured the settling time of a series of increasing order of filters, generated by cascading identical high pass biquads. Thus, we measured first a filter of second order, then a filter of 4^{th} order, built by two biquads, afterwards a 6^{th}-order filter by three identical biquads, and so on up to a filter of 20^{th} order, built by ten cascaded biquads. For each of these filters the settling time was measured with varying corner frequencies. A quality factor of Q=0.707 was used. Fig. 3.25 shows the measured data, the curve with the biggest settling time values correspondents to the system of 20^{th} order and that with the smallest value to the 2^{nd} order-filter.

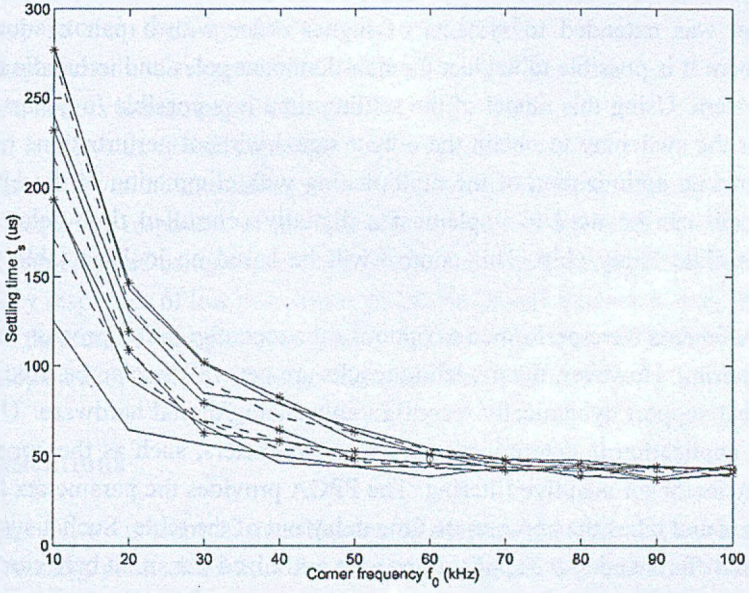


Fig. 3.25. Settling behavior of cascaded filters (Q=0.707) from 2^{nd} up to 20^{th} – order (lowest curve is one biquad, and successively highest is ten biquads)

Rys. 3.25. Czas ustalania w kaskadzie filtrów (Q=0.707) od drugiego do dwudziestego rzędu (najniższa krzywa dla jednej dwubiegunowej funkcji przejścia filtra i kolejno do najwyższej krzywej, dla dziesięciu funkcji przejścia)

This graph shows that the settling time of a system is, as in a 2^{nd}-order system, proportional to the reciprocal value of the corner frequency and differs from filters of smaller order with an offset. This is analogous to the modeling of the settling time of 2^{nd}-order systems. Additional measurements with different quality factors showed the same result with regard to the shape of the curve.

3.5.3. Concluding Remarks

This section presents an experimental model validation for dynamic reconfiguration of adaptive analog system (reconfigurable filter) using parallel Field Programmable Analog Arrays and switched multiplexer controlled by a mixed-mode system. Switching perturbations were analyzed and explained. In order to minimize the effects of these perturbations, analytical investigations of settling behavior for filters of 2^{nd} order were performed. A model for a time delay associated with the transitions due to the switching after the reconfiguration was established. It is shown that this model can be used for determination of the time delay which, can be used for optimization of dynamic reconfiguration. The model for the time delay was confirmed by measurements of all types of biquad filters. Measurements of cascaded systems show that the behavior of the settling time with respect to changes of the characteristic values, the corner frequency and the quality factor, is analogous, to that of a biquad filter.

The model was extended to systems of higher order with a pair of dominant poles [ZnPR02], where it is possible to neglect the non-dominant poles and to handle the system as a 2^{nd}-order system. Using this model of the settling time it is possible to generate the proper time delay for the switching to obtain the output signal without perturbations resulting from transients. For time optimization of the multiplexing with elimination of the effects of transient, this model can be used to implement a digitally controlled time delay into a Field Programmable Gate Array chip. This control will be based on look-up table stored in the FPGA.

These experiments were performed to optimize the reconfiguration process in applications of adaptive filtering. However, the modeling results are general and can be used in constructing systems that support dynamically reconfigurable analog/digital hardware. The time delay for an FPAA application is determined by proper parameters, such as the corner frequency and the quality factor for adaptive filtering. The FPGA provides the parameters for the reconfigured function and takes the appropriate time delay out of the table. Such a system provides for a variety of different adaptive applications with optimized transition behavior.

The performed experiments present the results of reports research aiming at construction of dynamically reconfigurable mixed-signal systems. Such systems are applicable in adaptive control, adaptive filtering, plant simulation, fault tolerant processing, and processing with minimization of power dissipated by the hardware. The last consideration, power minimization, is becoming critical in modern portable systems. Power optimization in a mixed-signal

system requires suitable assignment of tasks to analog and digital parts of the system. Typically digital processing is used for high complexity tasks with rather low frequency of operation while the analog processing is used for high frequency operation at rather low complexity. Digital processing dissipates substantially more power than the analog counterpart [Vitt90]. In addition the analog implementation is also very efficient in terms of required silicon area. The experiments performed at the University of Arizona and reported in [PGMP99a-b] showed that a typical filter implementation using a FPGA chip (XC4005XL [Xili98]) required 5 times the silicon area that was needed for implementation of corresponding filter implemented in the MPAA020 chip from Motorola. Consequently the task assignment should be directed by an effort to maximize the utilization of analog hardware subject to constraints in the form of complexity and required accuracy. The task assignment may change dynamically when processing requirements change or when a fault in some part of the system is detected. Such processing must be implemented in dynamically reconfigurable hardware.

The quality of reconfigurable filters constructed using the FPAA depends on: a) quality of capacitor banks, b) quality of amplifiers, c) chip manufacturing errors, and the dynamics of switching circuits in CAB environment [PaZn00]. In our experimental tests we used the MPAA020 chip [Birk98].

Some specific results of testing were:

- capacitor bank relative linearity errors (ε_r)
  a) for capacitors in the range $10u<C<40u$ $|\varepsilon_r|<0.1$,
  b) for capacitors in the range $40u<C<120u$ $|\varepsilon_r|<0.02$,
  c) for capacitors in the range $120u<C$ $|\varepsilon_r|<0.01$,
  where u is the value of unit capacitor in the capacitor bank,
- manufacturing variations – differences between the chip cells, relative errors measured in the frequency responses of the identical low pass filters with cut-off frequency of 20kHz implemented using various cells of the chip were less that 0.01 up to 200kHz,
- frequency responses of low pass filters of 20kHz cut-off frequency were compared with the theoretical (computed) responses and the relative errors in the operating frequency band (100kHz – 200kHz) were less than 0.01.

3.6. Applications

In this paragraph we present an investigation of dynamically reconfigurable mixed-signal circuits implementing plant simulators for predictive control and adaptive controllers. Motorola MPAA020 and Anadigm AN10E40 FPAA chips described in [Moto97a-d, Anad01a-d] and Appendix III, are used to build adaptive controllers and plant simulators for predictive control. The reported experimental studies describe performance and programmability of the field programmable analog array necessary for application in adaptive control and simulation. The experimental structure is based on two parallel FPAA chips, analog multiplexer and mul-

tiplexer's control logic, which is steered by a digital system such as a desktop computer or a FPGA chip. Dynamic reconfiguration is used in this system for adaptive control or adaptive processing in general. Modeling and measurements of the transitions in the internal blocks of the two FPAA chips working in parallel, and analysis of limitations resulting from hardware imperfections are presented [ZnPV04, PVZH01].

3.6.1. Reconfigurable Plant Simulator for Predictive Control

Predictive control uses a plant simulator, which is used to simulate the plant in "fast" time scale in order to anticipate the plant behavior and develop suitable control signals. Plant may operate in different regimes, which are described by suitable small signal models. Consequently the plant simulator has to have capability of adjustment, i.e. downloading proper models.

Assuming that the plant is described by the differential equations:

$$\begin{aligned} x(t) &= x(t_0) + \int_{t_0}^{t} f(x(\tau), u(\tau))\, d\tau \\ y(t) &= g(x(t), u(t)), \end{aligned} \tag{3.23}$$

where $x(t)$ - state variable, $y(t)$ - output variable, $u(t)$ - input variable, and $x(t_0)$ is an initial condition at a time t_0, then the simulator can be constructed using the FPAA. However, standard FPAA (MPAA020) does not have the tracking capability, which is necessary for inputting proper initial conditions before the simulation. In this section we discuss modification to FPAA implemented using an external circuitry to accomplish tracking operation. Operation of model downloading sequence is illustrated in Figs. 3.26a and b.

The FPAA runs as a dynamic system with configuration and parameters both set on-the-fly. Those settable elements can be downloaded to the chip in a time interval not shorter then the time of downloading T_p (Fig. 3.26b). During the downloading time the analog outputs are forced to the zero voltages [Moto97a, Moto97c]. At the end of the interval T_p, the chip starts to perform its designated function. Thus, when the circuit is supposed to work as a reconfigurable continuous dynamic system it is necessary to use FPAA's working in parallel. This is because the valid output signal is generated by the FPAA only between consecutive downloading sequences.

In order to assure proper operations from initial time t_0 to the actual time t and to fulfill Eq. (3.23), the entire system has to work as a parallel FPAA set alternatively downloaded.

It is required that the actually working part is tracked by newly downloaded part. In the next step, when working part starts to reload, the tracking part will start processing with proper initial conditions. This is necessary only for a state variable x in Eq. (3.23). The indicated parts of the system i.e. *Part1* and *Part2* fulfill this condition of switching the state variable x, using the control signals *R1* and *R2*. These signals force the two modes of the integrators in the FPAA structures: *initial condition (track)* mode (*R1*=1, *R2*=1) and *compute (integrate)* mode (*R1*=0, *R2*=0). Functions f and g can be computed by the control computer and downloaded to the FPAA chip

system in consecutive phases in the form of a new configuration. The output variable $y(t)$ from analog multiplexer controlled by Control logic module (signal $\underline{A}$), is an output variable of FPAA dynamic plant simulator.

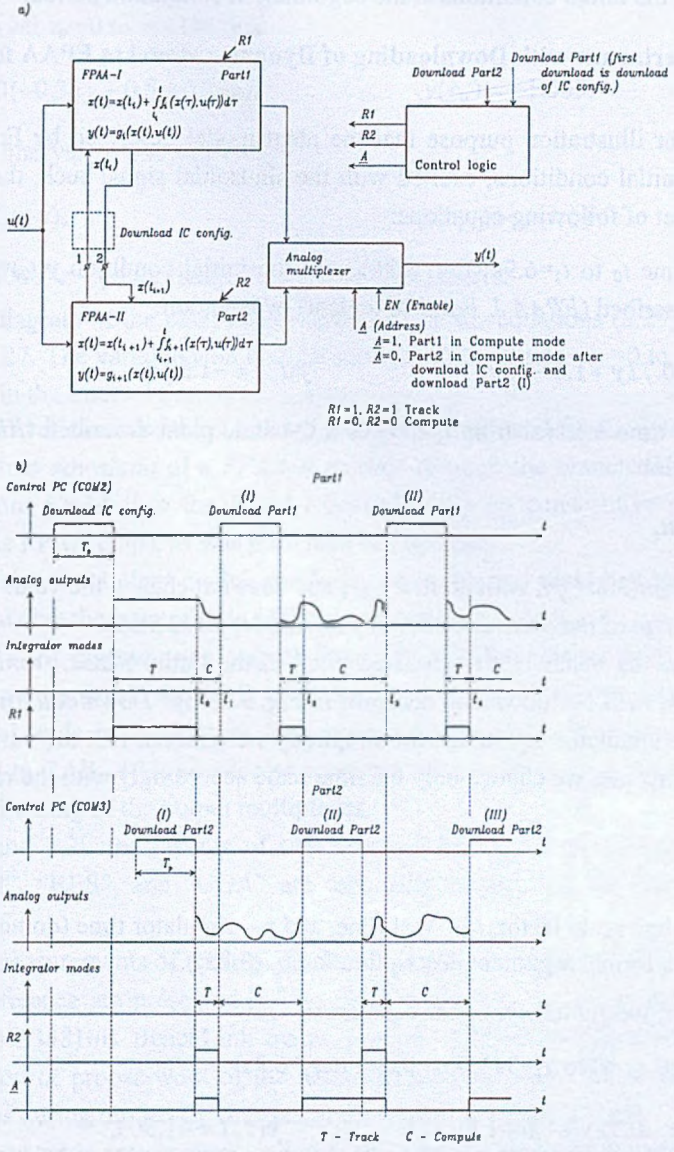


Fig. 3.26. Dynamic plant simulator based on operation of two parallel FPAA: a) diagram, b) time sequences (timing specification)

Rys. 3.26. Symulator obiektowy bazujący na dwu współpracujących równolegle układach FPAA: a) schemat blokowy, b) sekwencja czasowa (specyfikacja sekwencji sterującej)

In the experimental station, the implementation of the plant simulator (3.23) has used two FPAAs with *track/compute* capability [PaZn00, PaZn01], the analog multiplexer similar to the Siliconix DG408 [Maxi01, Temi97] and one FPGA for Control logic implementation. Symbol $x(t_i)$ represents the initial conditions at the beginning of simulation period.

3.6.2. Experiments with Downloading of Dynamic Model to FPAA for Plant Simulator

Consider for illustration purpose that the plant model described by Eq. (3.23) is linear, starting from initial conditions, excited with the sinusoidal signal such, that it can be represented by the set of following equations:

from the time t_0 to t_1=6.9s (Fig. 3.26) with the initial condition $y(t_0)$= −1.503, as a dynamic plant described (*FPAA-I, Part1* of a plant) by equation:

$$\frac{dy}{dt} = -0.72y + 1.0 - 1.5u, \qquad y(t_0) = -1.503, \tag{3.24}$$

in the next time interval from t_1 to t_2 as a dynamic plant described (*FPAA-II, Part2* of a plant) by equation:

$$\frac{dy}{dt} = -u, \tag{3.25}$$

where u=1·sin(3.8t+φ), with arbitrary φ, and does not change the value of a state variable y when the change of the plant equation in a moment t_1 takes place.

We validate the behavior of simulated plant in the initial phase: from initial conditions through the first *FPAA-II* download designed in Fig. 3.26 by "*Download Part2 (I)*".

To find the simulator equations, for simplicity we assume, that the variable scale factors are equal to unity, and we change only the time scale accordingly with the relation:

$$a_t = \frac{\tau}{t} \tag{3.26}$$

where:

a_t – time scale factor, t – real time, and τ– simulator time (do not confuse with a formal argument description in Eq. (3.23)).

Using (3.26) we get the simulator equations:

interval time τ_0 =0 to τ_1=345.0μs (t_0 =0 to t_1=6.9s)

$$a_t \frac{dy}{d\tau} = -0.72y + 1.0 - 1.5u, \qquad y(\tau_0) = -1.503, \tag{3.27}$$

interval time τ_1=345.0μs to τ_2 (t_1 =6.9s to t_2)

$$a_t \frac{dy}{d\tau} = -u, \text{ with continuous state vector } y, \tag{3.28}$$

where $u = 1 \cdot \sin(3.8 \cdot \frac{1}{a_t} \cdot \tau + \varphi)$.

The reference voltage in MPAA020 is equal to 2.5V. The bandwidth of the elements admit the slew rate up to 10V/μs [Moto97d] so we can use e.g. a_f=0.00005. In the experiment we have speed-up in simulation 20000 times.

The simulator equations after the time and amplitude scaling have a final form (in volts):

in the time interval τ_0 =0 to τ_1=345.0μs

$$\frac{dy}{d\tau} = 40000(-0.36y + 0.5 - 0.75u), \qquad y(\tau_0) = -1.503, \tag{3.29}$$

and in the time interval τ_1=345.0μs to τ_2

$$\frac{dy}{d\tau} = 20000(-u), \qquad y(\tau_{1,+}) = y(\tau_{1,-}) \tag{3.30}$$

where $u = 1 \cdot \sin(76000 \cdot \tau + \varphi) = 1 \cdot \sin(2\pi f\tau + \varphi)$, and f=12.1kHz.

The simulator diagram of the plant model described by the equations (3.29) and (3.30) is presented in Fig. 3.27. The variable y on that diagram for interval time τ_0 =0 to τ_1=345.0μs is denoted by y_1, and in the interval time τ_1 to τ_2, by y_2 .

Experiments and validation of the simulated plant was performed for the *initial conditions* mode and consecutive *download* of a *FPAA-II* module through the branch *D1Z*, copying of the state vector from *FPAA-II* to the *FPAA-I* depends only on consecutive configurations downloaded into the FPAA chips, as was presented in Fig. 3.26.

The predictive simulated plant model, can be tuned to the real plant just by external signals, which can actualize the current state of the simulated plant model.

Wires *D3X* and *D2X* represent the outputs from FPAA to the external switches fulfilling the fast change of modes inside the CAB of FPAA. *DP1* and *DP2* signals from FPAA synchronize the control logic of the system. The signals *R1* and *R2* control the mode control switches connected to CAB. *A0* is an address accompanying mode control signals *R1* and *R2* in sequential re-addressing of the output multiplexer.

In Figs. 3.28 and 3.29 the layouts of two separate FPAA are presented. The macros "Intgrp1", "Intgrp2", "RES", and "UGA" are especially constructed for experiments with plant simulator.

The results of measurements of analog signals, control logic signals and a transient waveforms in mutual reference are presented in Figs. 3.30 through 3.33. The scope screens were downloaded with HP34810B BenchLink Scope program [HePa96]. The goal of measurements was validation of proper work of the reconfigurable simulator and evaluation of dynamic imperfections during on-the-fly changes of the modes in FPAA's CAB.

The exciting sinusoid is not synchronized with the start and finish of download processes, there is only one run of the signals during all download sequence (compare waveforms from Fig. 3.30 with Fig. 3.33, and waveforms from Fig. 3.30 with waveforms from Figs. 3.31 and 3.32).

The triggering in measurements is caused by constant DC macro in *Part2* of the system (Figs. 3.27 and 3.26) signaling the end of the download process.

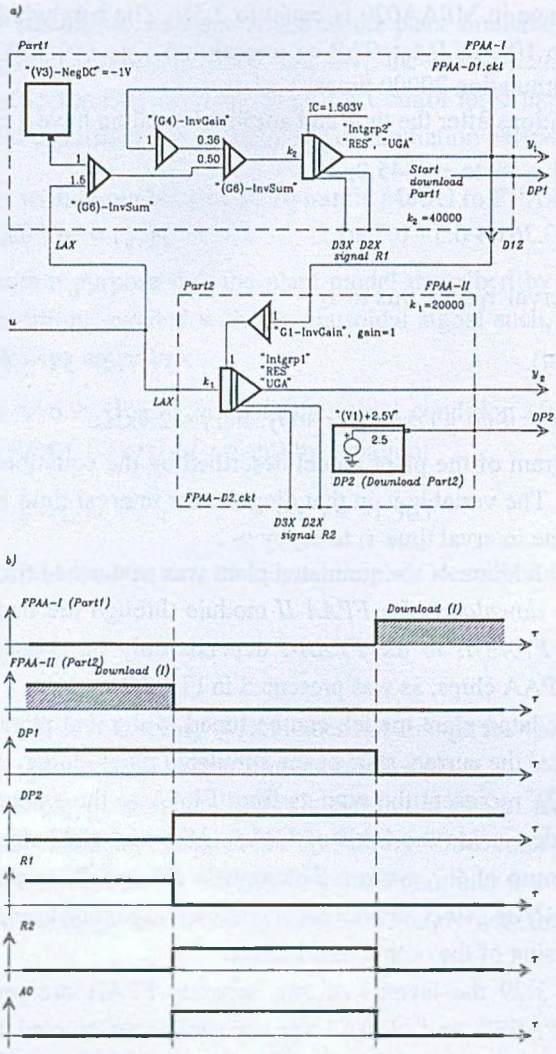


Fig. 3.27. FPAA implementation of plant linear model: a) diagram implemented in two MPAA3BRD Evaluation Boards [Moto97c], b) control timing for the transient state in the change of modes between two FPAA

Rys. 3.27. Implementacja w technologii FPAA obiektu liniowego: a) schemat dla dwu obwodów drukowanych MPAA3BRD [Moto97c], b) sekwencja czasowa sterowania stanami nieustalonymi spowodowanymi zmianą stanów współpracujących FPAA

The next phases of simulation and vector state rewriting depends on start of its rising edge. In Fig. 3.30 this signal is viewed in channel 3, and the end of *FPAA-II* downloading is signed by a symbol A. The second triggering waveform signalizes start of downloading of *Part1* (next after *Part2*) of the system (Point B in Fig. 3.30 at 345.0μs, and details in Fig. 3.32).

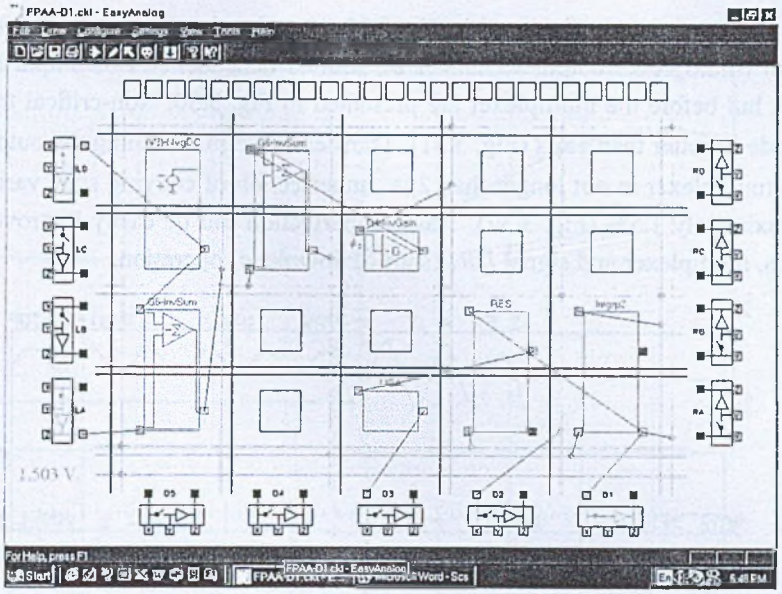


Fig. 3.28. Plant simulator: layout of the *FPAA-I Part1* implementing relation (3.29)
Rys. 3.28. Symulator obiektowy: pole łączeń *FPAA-I Part1* implementujące relację (3.29)

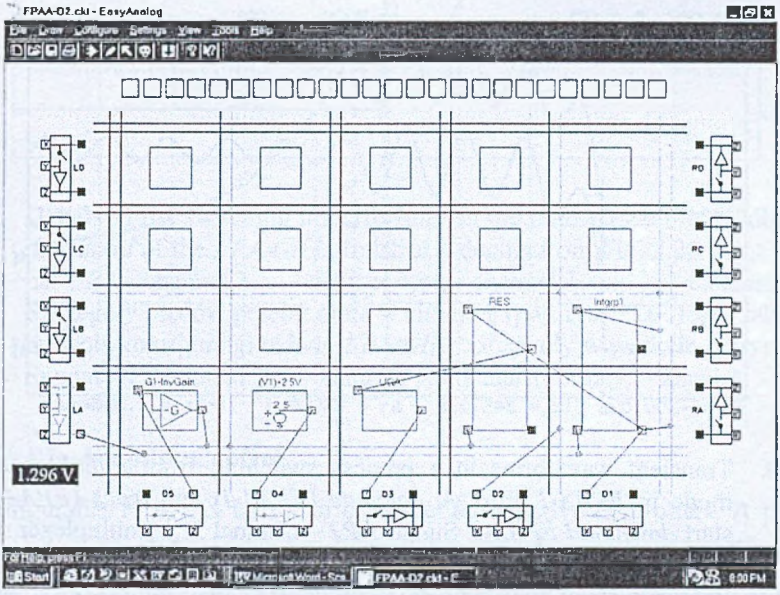


Fig. 3.29. Plant simulator: layout of the *FPAA-II Part2* implementing relation (3.30)
Rys. 3.29. Symulator obiektowy: pole łączeń *FPAA-II Part2* implementujące relację (3.30)

The input of the plant is displayed in Fig. 3.33 (sine signal - channel 1) in reference to the plant output (multiplexer output - channel 2). Mutual dependencies of output signals from both FPAA but before the multiplexer are presented in Fig. 3.30. Non-critical transient state in track mode is better then 15μs (Fig. 3.31). Transient state in switching the output signals in FPAA and multiplexer in not longer than 2μs. Imperfection of copying state variable reaches value approximately 1.5% (Fig. 3.32). These imperfection can be easily improved by tuning the switches, multiplexer and signal *DP1* (start of download) operation.

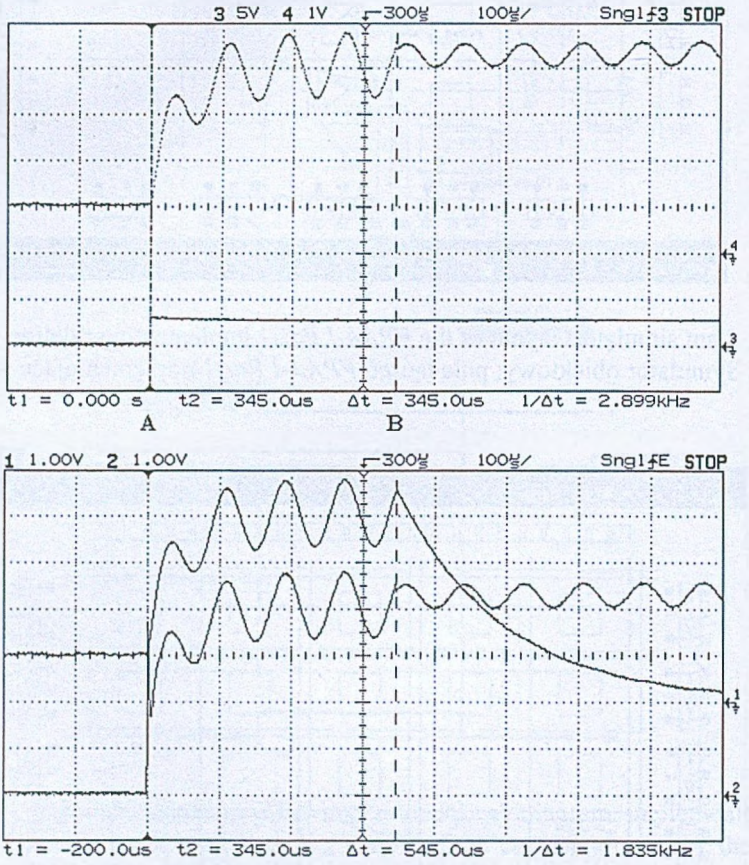


Fig. 3.30. Transient waveforms in a process switching from *initial conditions* mode in *FPAA-I*, through *compute* (*FPAA-I*) and *track* (*FPAA-II*) to start *download FPAA-I*. Signal *DP2* – channel 3, *y* (multiplexer output, see Fig. 3.26a) – channel 4, y_1 – channel 1, and y_2 – channel 2

Rys. 3.30. Przebiegi stanu nieustalonego w procesie przełączania *FPAA-I* ze stanu *warunki początkowe*, poprzez *liczenie* (*FPAA-I*) i *śledzenie* (*FPAA-II*) do rozpoczęcia wpisu konfiguracji do układu *FPAA-I*. Sygnał *DP2* – kanał 3, *y* (wyjście multipleksera, por. rys. 3.26a) – kanał 4, y_1 – kanał 1, oraz y_2 – kanał 2

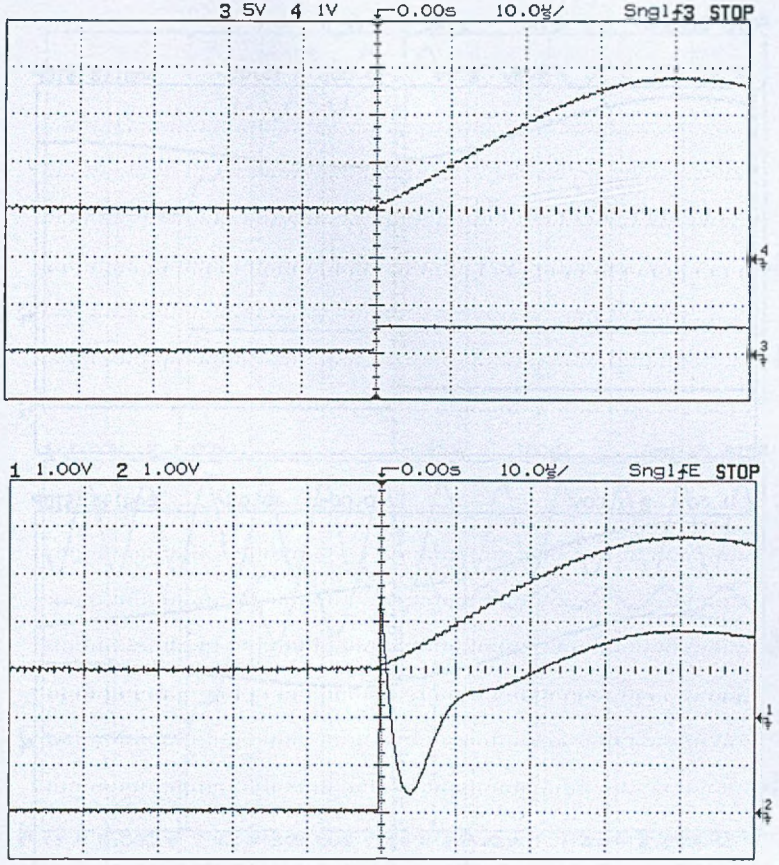


Fig. 3.31. Details of the switching imperfections in the time t_0 (see Fig. 3.26b) when *download* of the *FPAA-II* is finished – details from Fig. 3.30 point A. Signal *DP2* – channel 3, y – channel 4, y_1 – channel 1, and y_2 – channel 2

Rys. 3.31. Szczegóły błędów przełączania w chwili t_0 (por. rys. 3.26b) gdy zakończono wpis konfiguracji układu *FPAA-II* – szczegóły w punkcie A (rys. 3.30). Sygnał *DP2* – kanał 3, y – kanał 4, y_1 – kanał 1, oraz y_2 – kanał 2

3.6.3. FPAA in Adaptive Control

The reconfigurable FPAA is useful in constructing adaptive controllers. A plant is described by the set of coupled transfer functions. These transfer functions are determined for specific operating conditions (e.g. input flow and liquid state), which must be modified when operating conditions change.

Based on the interaction of the transfer functions, it is necessary to design controllers which decouple e.g. the two variables in the controlled system. The transfer functions change the parameter values depending on the operating point and may also change their structural

form. This may result in loss of decoupling operation in control system and may lead to instabilities.

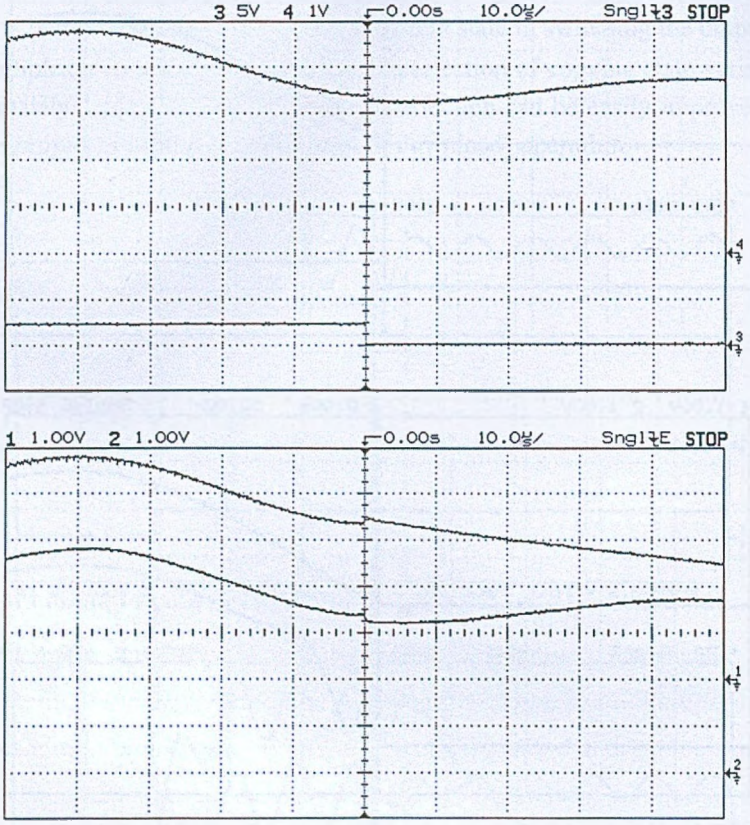


Fig. 3.32. Details of switching spikes in point B (Fig. 3.30) at the start of *download* of *FPAA-I* (signal *DP1*- channel 3). y – channel 4, y_1 – channel 1, and y_2 – channel 2

Rys. 3.32. Szczegóły przełączania w punkcie B (rys. 3.30) w chwili rozpoczęcia wpisu konfiguracji układu *FPAA-I* (sygnał *DP1*- kanał 3). y – kanał 4, y_1 – kanał 1, oraz y_2 – kanał 2

Consequently the controller has to be adapted to the changes in plant temperature and fluid states to assure decoupling of the two control loops in all regimes. Suitable plant models are stored in flash memory and are downloaded depending on detected temperature and fluid level ranges. The controller can be constructed using the FPAA. The controller transmittances can be simply implemented into FPAA chip using standard library or user-defined macros.

An example of FPAA adaptive controller is shown in Fig. 3.36. The controlled system is a distillation column presented in a simplified schematics in Fig. 3.34.

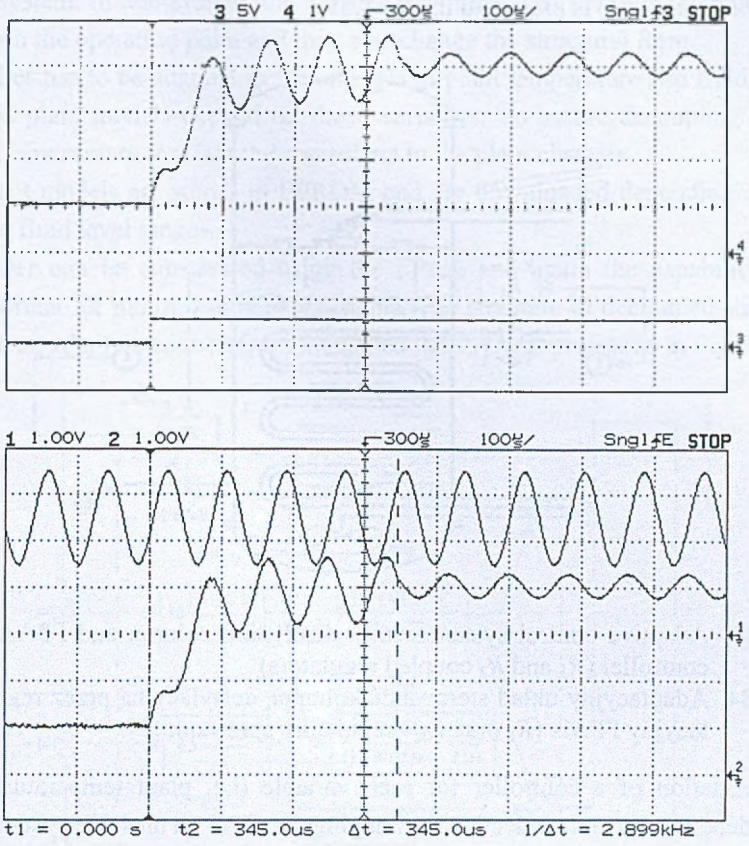


Fig. 3.33. The system input/output/control signals. Multiplexer output (channel 4 and 2) vs. end of *download* of *Part2 (FPAA-II) DP2* signal (channel 3), *u* – channel 1

Rys. 3.33. Sygnały wejście/wyjście/sterowanie systemu. Wyjście multipleksera (kanał 4 i 2) w odniesieniu do sygnału *DP2* (koniec wpisu konfiguracji w układ *Part2 (FPAA-II)* – kanał 3), *u* – kanał 1

The object (controlled system – distillation column) is described [Dorn98, Schw61] by the set of coupled transfer functions:

$$\begin{aligned} x_1 &= \frac{1}{(1+0.025s)^3} y_1 + \frac{1}{(1+0.025s)\cdot(1+0.1s)} y_2 \\ x_2 &= -\frac{1}{(1+0.025s)^2} y_1 + \frac{1}{(1+0.025s)\cdot(1+0.1s)^2} y_2 \end{aligned} \tag{3.31}$$

These transfer functions are determined for a specific operating conditions (input flow and liquid level in the column). When the operating conditions change the plant behavior is de-

scribed by different set of transfer functions. Structure of a two-dimensional controlled system based on Eqs. (3.31) is presented in Fig. 3.35.

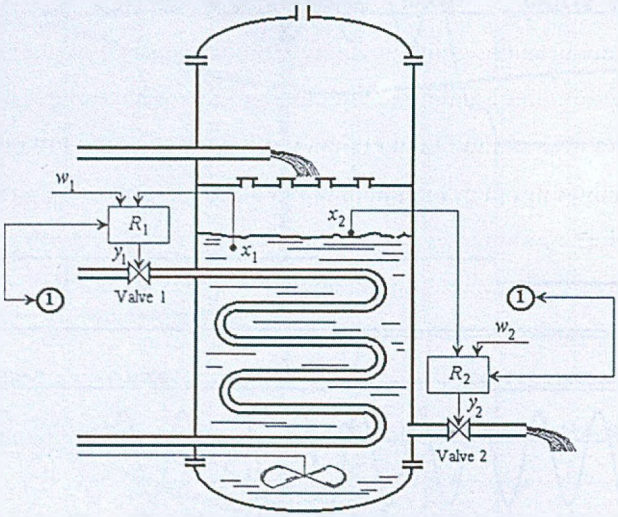


Fig. 3.34. Adaptive control system with a distillation column and FPAA's adaptive controller (R_1 and R_2 coupled regulators)

Rys. 3.34. Adaptacyjny układ sterowania kolumną destylacyjną przez regulator adaptacyjny FPAA (R_1 oraz R_2 – regulatory sprzężone)

Implementation of a controller for each variable (i.e. plant temperature x_1, and fluid level x_2) independently and neglecting the coupling, leads to an unstable system [Dorn98].

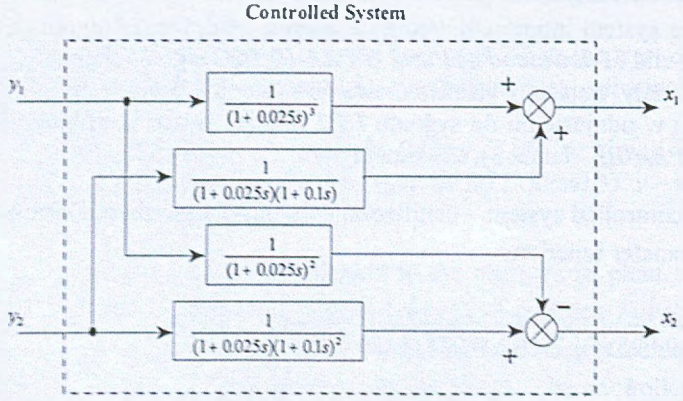


Fig. 3.35. Structure of a two-dimensional controlled system: example of transfer functions for one operating point

Rys. 3.35. Struktura dwuwymiarowego układu sterowania: przykład funkcji przejścia dla wybranego punktu pracy

Therefore, it is necessary to design controllers, which would decouple the two variables in the controlled system. In real system, the transfer functions (3.31) change the parameter values depending on the operating point and may also change the structural form.

The controller has to be adapted to the changes in plant temperature and fluid levels, because linearized plant models depend on those variables. To assure decoupling of the two control loops it is necessary to adapt the controllers to the plant changes.

Suitable plant models are stored in EPROM and are downloaded depending on detected temperature and fluid level ranges.

The controller can be constructed using the FPAA and again the capability of signal tracking is important for minimization of transients. The structure of decoupled adaptive control system with an adaptive controller implemented in FPAA, is presented in Fig. 3.36.

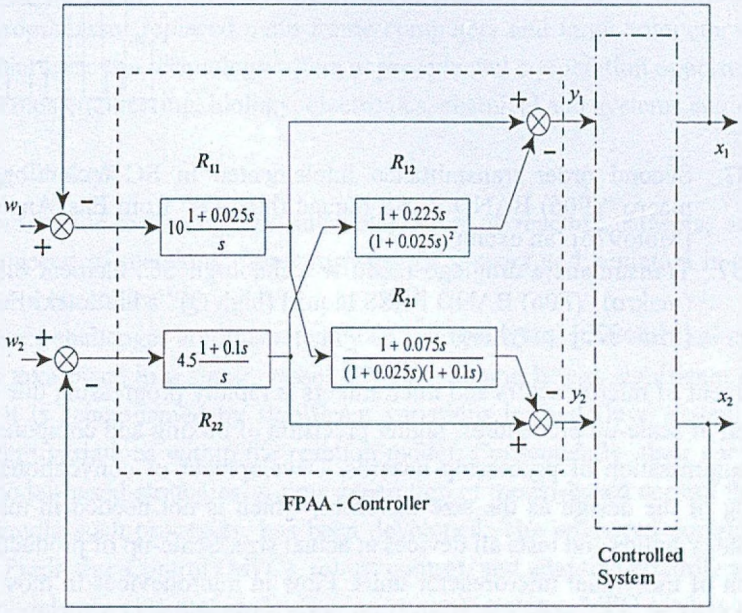


Fig. 3.36. Structure of decoupled control system for the example plant model
Rys. 3.36. Struktura odsprzężonego układu sterowania dla przykładowego modelu obiektu

The controller transmittances can be simply implemented into FPAA chip using standard libraries' macros or user defined macros [PaZn00, PaZn01]. As an example, a second order transmittance implemented in SC technology is presented in Fig. 3.37.

3.6.4. Adaptive FPAA Controllers for Microreactors

Field Programmable Analog Arrays, coupled with microreactor technology promise to change the way plants are built, as well as the methods by which their processes are designed and controlled.

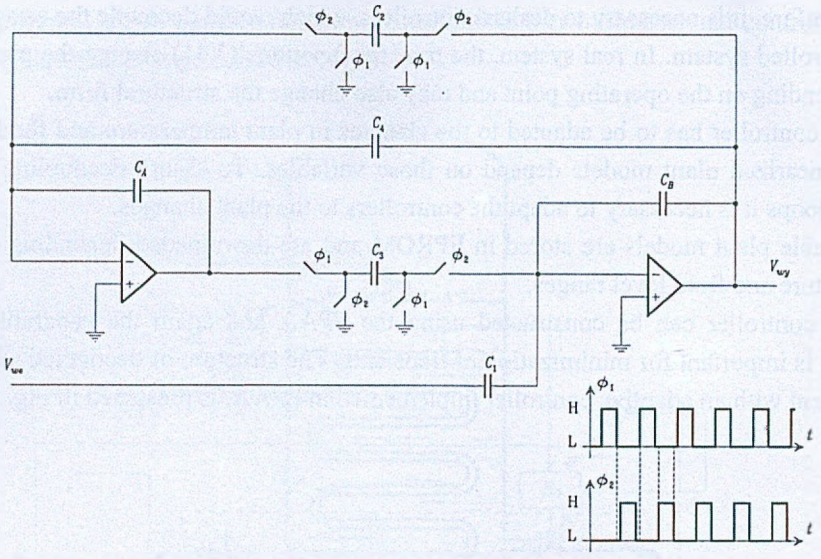


Fig. 3.37. Second order transmittance implemented in SC technology, library macro "(F06) BAND PASS biquad (high Q)" from EasyAnalog library [Moto97b] (an example)

Rys. 3.37. Transmitancja drugiego rzędu w technologii SC, element biblioteczny (makro) "(F06) BAND PASS biquad (high Q)" z biblioteki EasyAnalog [Moto97b] (przykład)

Development of microreactors and micromixers is rapidly progressing due to factors such as elimination of scale-up procedures, higher precision of mixing and component contact surfaces, and minimization of processing hazards. Development of conventional hardware requires scaling of the design as the size increases, which is not needed in microtechnology. Microtechnology builds and tests all devices at actual size. Scale-up of production is achieved by replication of individual microreactor units. Flow in microdevices in most cases remains laminar. The vast majority of mixing devices rely on diffusion, which occurs between fluid layers. Due to the laminar flow, large contact surfaces between components and small microdevice dimensions induce very small diffusional paths. These short diffusion paths give the benefit of reducing the time, with demonstrated speeds in the range of a few milliseconds to as fast as few microseconds [Caru00]. Miniaturization of reactors provides inherent safety, because it lessens the consequences of potential mishaps via reduction of hazardous inventories, reactor volumes and pipe diameters. Another significant effect of device miniaturization is dramatic speed-up of processes, which imposes pressure on development and design of very fast sensors, actuators and controllers. In addition, the use of microreactors allows for reduction of expensive reagents, fluidic components with dead volumes, integration of sensors and actuators and parallel screening. The reduction in size and integration of multiple functions create structures with capabilities exceeding those of conventional macroscopic

systems, and provide for means to lower costs, while improving safety and production. Integrated heaters and sensors, combined with lower thermal mass of enclosures, can yield significant improvements in response times. Examples of microreactor applications include chemical analysis, customized synthesis, combinatorial synthesis of drugs, nucleic acid detection and synthesis etc. [MaBe98]. DuPont has synthesized several hazardous chemicals in a microreactor built using joined silicon wafers with microfabricated channels, catalytic reactor sections, and preheaters [LHRA96].

Microreactor technology and the ability it gives to reproduce complex designs in parallel component processes will lead to innovative designs and changes in manufacturing technology. New reaction pathways will be invented with environmentally benign solutions to chemical manufacturing. The large scale manufacturing of individual components and subsequent integration will replace existing large plants by numerous smaller, distributed facilities, just as the microprocessor replaced main frame computers and large computer centers. The realization of microreaction technology offers unprecedented cooperation opportunities across chemistry, materials engineering, biology, electronics, chemical and systems engineering.

Challenging Controls

While microreactor technology permits integration of reactors, sensors, actuators and controllers, the speed of reactions, faster response of sensors and actuators is creating new challenges for process control.

Process control challenges are illustrated by an example of reactive distillation, where two unit operations take place in a single vessel. This processing brings significant cost savings [KeBr00], but it is accompanied by significant variations in feed flow, system's residence time and resulting variations within the reaction model. Consequently, their control requires sophisticated model-based-strategies. A new generation of model-based control theory, which is tailored to handle such processes, has been developed. The advanced control algorithms include Model Predictive Control (MPC), robust control, and adaptive control, where mathematical plant models are essential in developing control strategy. MPC models may have to run 50-500 times faster than real time. The implementation of MPC was effective in solving large, multi-parameter industrial control problems [QiBa97]. Requirements for computing power and speed in MPC applications are substantial and will increase with microreactor technology. It is anticipated that high quality control, such as provided by MPC, will have significant impact on manufacturing. Controllers will be adaptive and self-tuning, with optimization of operating conditions, and controls will be hierarchical and distributed. Fault detection algorithms will be also employed to deal with control and process abnormalities.

Traditional analog circuits do not provide the capability of changing circuits once constructed. However, the combination of the new technology of Field Programmable Analog Arrays with the more commonly used technology of Field Programmable Gate Arrays, provides a basis for the development of dynamically reconfigurable analog/digital hardware.

As FPGA's are devices providing for the implementation of digital functions created using a software-based, high-level digital design approach, FPAA's enable the implementation of analog functions created through software-based, high-level analog design. By using two or more FPAA's in parallel, it is possible to reprogram the system and reassign the circuits in real time. Dynamically reprogrammable controllers for microreactors can adapt to changing process parameters whose force the changes in the plant operating point. Proper switching of the FPAA outputs may provide an uninterrupted processing of the input signal. To optimize the transitions of the switching and speed the controller reconfiguration process, it is necessary to analyze the dynamic behavior of the reconfiguration and to model the transitions between the diverse chips in an experimental setup [PVZH01].

3.6.5. Switching in Adaptive FPAA Controllers

An experiment was performed to validate the behavior of adaptive controller in continuous mode operation. The test set was built using two DS's (Development System [Anad01c]) for implementation of different transfer function and some external control logic. The DS contains a single AN10E40 array and an MC68HC908GP32 microcontroller.

AnadigmDesigner [Anad01a] provides for communication with four flash memory locations in the microcontroller or direct programming of the array during powered operation. Communication with the board is via an RS-232 connection between the PC and the DS. The four flash memories can be activated by a switch, allowing these memory locations to act as a buffer for implementing one possible version of a rapidly reconfigurable system. Time of downloading from the serial port is approximately equals to 2s, while from flash memory is 30ms.

In the experiment we have used one bit for addressing desirable flash memory containing one of two proper configurations to simulate an operation typical for adaptive controller in fast reconfiguration mode. Using 3 bit address for two DS's, we can get one of eight desired configurations saved in the flash memories. It should be stated, that inactive flash memory can be reloaded through the RS-232 port from PC during continuous work of controller, so the number of possible configuration files is unlimited

In the experiment, one FPAA (FPAA1) is programmed to implement a 4-th order low-pass filter described by the transfer function:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{(1+Ts)^4},$$

where T is the time constant. In the implemented circuit it was assumed, that T equals to $100 \cdot 10^{-6}$ sec., so that the transfer function for FPAA1 is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{(1+100 \cdot 10^{-6} s)^4}.$$

This circuit implementing this function is shown in Fig. 3.38.

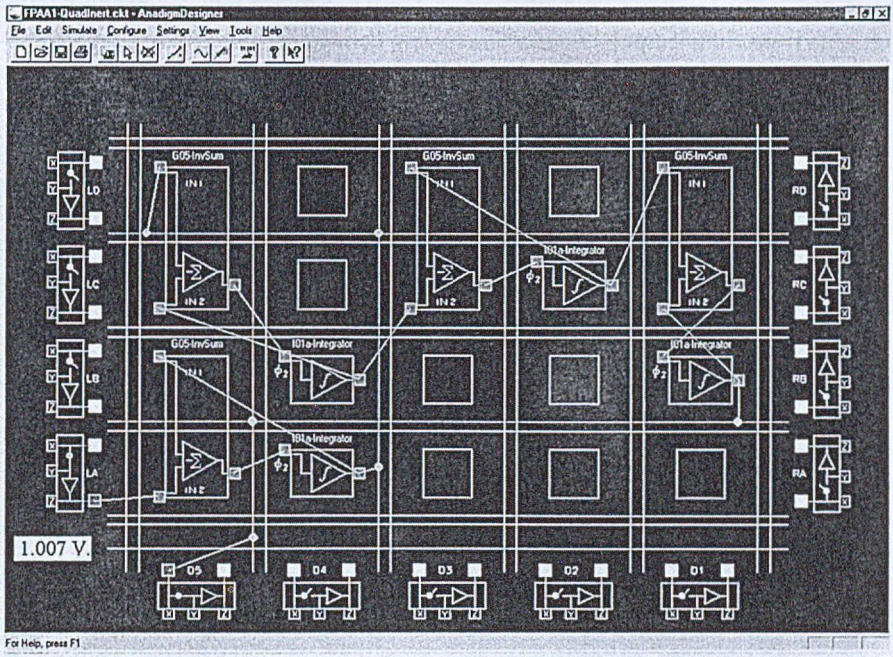


Fig. 3.38. 4th order low-pass filter Analog Array circuit
Rys. 3.38. Struktura połączeń filtru dolnoprzepustowego czwartego rzędu w FPAA

The second FPAA (FPAA2) is used to implement a band-pass filter with the transfer function given below

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{2\pi f_0 \frac{G}{Q} s}{s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2},$$

where:

G – pass-band gain (center frequency gain), f_0 – center frequency, and Q – quality factor.

The center frequency was assumed equal to 4kHz, the pass-band gain assigned was 2, and the chosen quality factor was of value 4. For these values of parameters we have the transfer function of the band-pass filter in a form:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{12.57 \cdot 10^3 s}{s^2 + 6.28 \cdot 10^3 s + 631.65 \cdot 10^6}.$$

The circuit implementing this function (macros G01-InvGain and F06-BPHQ) is shown in Fig. 3.39.

The two FPAA's were alternately downloaded with programs implementing the 4-th order low-pass filter and band-pass filter to simulate an adaptive controller, changing the transfer

function in time. The inputs of both FPAA's were connected to the square input signal (system excitation) and their outputs were alternatively connected, via multiplexer, to the system output.

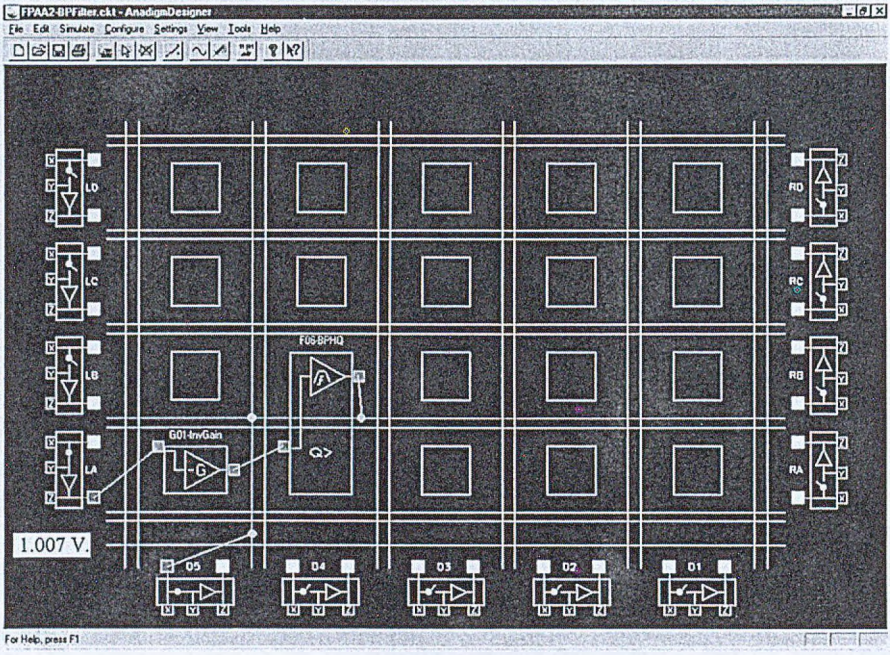


Fig. 3.39. Band-pass Filter Analog Array circuit
Rys. 3.39. Struktura połączeń filtru środkowo-przepustowego w FPAA

The results of measurements of analog signals, control logic signals and transient waveforms in the individual FPAA's and at the system input and output are presented in Figs. 3.40 through 3.43.

The transfer functions selected for alternative downloading of FPAA's differ by parameter values and filters structures. This selection was made to emphasize the differences between the two implementations, which allows us to magnify and conveniently observe switching imperfections. In most practical situations the transfer functions do not differ so drastically. Transfer functions in the decoupling controllers of two variable system distillation column [Dorn98] differ by transfer function parameters only. The structures of both controllers stabilizing the temperature and level of fluid remain constant during operation.

The oscilloscope screens were downloaded with HP34810B BenchLink Scope program [HePa96]. The goal of measurements was demonstration of implementation of reconfigurable controller with alternative transfer functions in AN10E and evaluation of dynamic imperfections during on-the-fly changes in the modes of FPAAs.

The experiments showed that the transfer function can be changed approximately 30 times per second. The transient state after download process is not longer than 2ms.

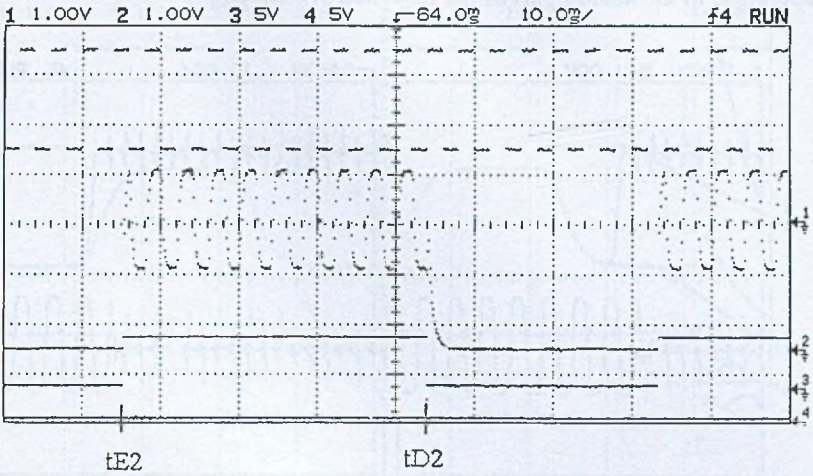


Fig. 3.40. Example of signal transitions during alternative downloading of the transfer functions to FPAAs in long time scale showing two intervals of downloading.
Description of channels: channel 1 – system input signal (square wave), channel 2 – output of FPAA1 implementing 4-th order low-pass filter, channel 3 – control signal (FPAA1 enable), channel 4 – control signal (start download of FPAA1 – for clarity of view the waveform amplitude is reduced 2 times).
tE2 – moment of time when download of FPAA1 is finished, tD2 – moment of time when download of FPAA1 is started (signal in channel 4)

Rys. 3.40. Przykład stanu przejściowego podczas przemiennego wpisu konfiguracji dla funkcji przejścia do układów FPAA w dłuższym odcinku czasu, ukazujący dwa interwały czasu wpisu konfiguracji.
Opis kanałów: kanał 1 – sygnał wejściowy systemu (fala prostokątna), kanał 2 – wyjście układu FPAA1 realizującego filtr dolnoprzepustowy czwartego rzędu, kanał 3 – sygnał sterujący (FPAA1 aktywny), kanał 4 – sygnał sterujący (start wpisu konfiguracji do układu FPAA1 – dla poprawy czytelności, amplitudę przebiegu zredukowano dwukrotnie).
tE2 – chwila w której zakończono wpis konfiguracji do układu FPAA1,
tD2 – chwila w której rozpoczęto wpis konfiguracji do układu FPAA1 (przebieg z kanału 4)

3.6.6. HDL Code Generation for Control Logic

The mixed-mode systems synthesis creates the problem of designing of the control logic for switching the analog and digital parts of the system accordingly to the timing resulting from the system specification [ZnPa00]. Analog part of the system can be realized in the ASIC technology through implementation of established analog-digital functions for signal processing (e.g. analog/digital, digital/analog, frequency/voltage conversion, multiplexing,

programmable gain control, audio, radio, automotive circuits) [Nati93, Temi97], FPAA technology [AMBA97, Moto97a, DMGu98, BrMa98, RZPV99] or standard cell structures for layout generation in the analog part of the designed system chip.

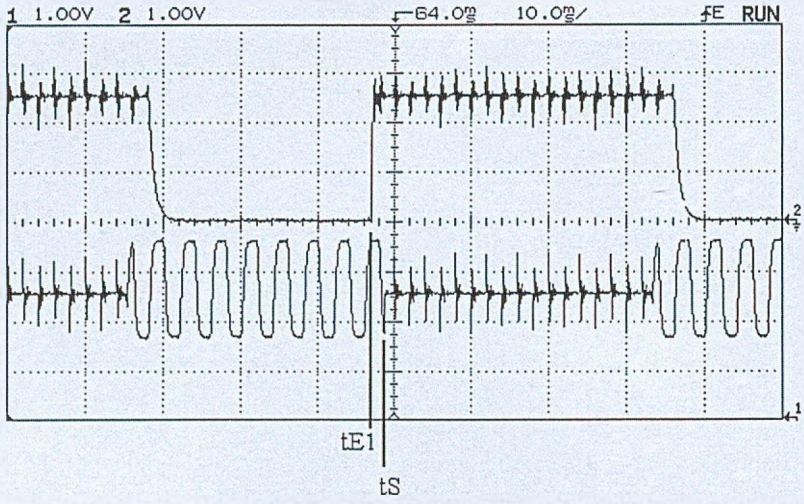


Fig. 3.41. Example of signal transitions (contd. Fig. 3.40) during alternative downloading of the transfer functions to FPAAs in long time scale showing two intervals of downloading.
Description of channels: channel 1 – system output signal, channel 2 – output of FPAA2 implementing band-pass filter.
tE1 – moment of time when download of FPAA2 is finished, tS – moment of switching when the system output switches from the 4-th order low-pass filter to the band-pass filter operation, (tS-tE1) – time interval hiding the transient in the band-pass filter after download. For AN10E40 the transient is shorter than 2ms, which is the worst case

Rys. 3.41. Przykład stanu przejściowego (kontynuacja rys. 3.40) podczas przemiennego wpisu konfiguracji dla funkcji przejścia do układów FPAA w dłuższym odcinku czasu, ukazujący dwa interwały czasu wpisu konfiguracji.
Opis kanałów: kanał 1 – sygnał wyjściowy systemu, kanał 2 – wyjście układu FPAA2 realizującego filtr środkowo-przepustowy.
tE1 – chwila w której zakończono wpis konfiguracji do układu FPAA2, tS – chwila przełączenia wyjścia systemu z filtru dolnoprzepustowego na filtr środkowo-przepustowy, (tS-tE1) – interwał czasu "ukrywający" stan przejściowy filtru środkowo-przepustowego po wpisaniu konfiguracji. Dla układu AN10E40 stan przejściowy jest nie dłuższy niż 2ms

The digital part of the mixed-mode system can be implemented depending on the used technology, in form of programmable logic like FPGA or CPLD [Xili98, Xili99], or, placed in the digital part of the mixed-mode layout of the designed chip. However, independently of the

technology applied, the logic connection defining the behavior of the mixed-mode system, establishes the system timing.

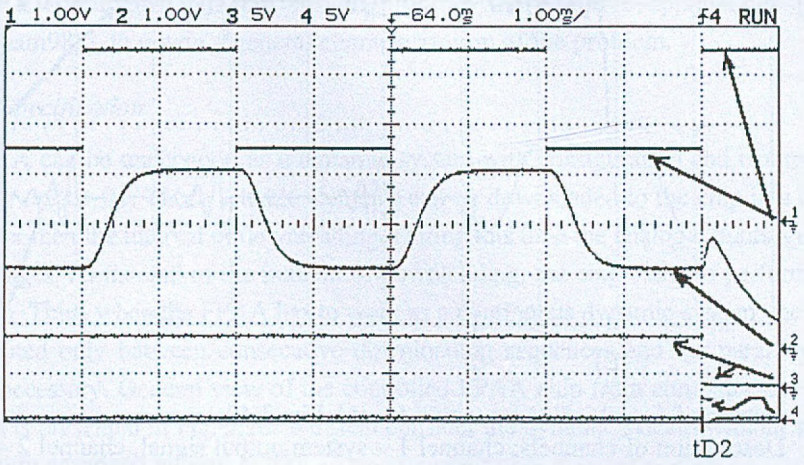


Fig. 3.42. Details of downloading transition.
Description of channels: channel 1 – system input signal (square wave), channel 2 – output of FPAA1 implementing 4-th order low-pass filter, channel 3 – control signal, channel 4 – control signal

Rys. 3.42. Szczegóły stanu przejściowego wpisu konfiguracji.
Opis kanałów: kanał 1 – sygnał wejściowy systemu (fala prostokątna), kanał 2 – wyście układu FPAA1 realizującego filtr dolnoprzepustowy czwartego rzędu, kanał 3 – sygnał sterujący, kanał 4 – sygnał sterujący

The system timing is applied to the determination of behavior of large collaborating part of the designed systems due to its objectivity and natural suitability to the formalization. Formal translation from the timing definition to its hardware implementation is done using Hardware Description Languages (HDL) VHDL or Verilog [IEEE94-95, ThMo91] in the intermediate phase preceding the implementation of the timing into the hardware.

This section presents, a translation process of the control timing specification in the mixed-mode system, to the HDL code. The formalization of timing diagram to its linguistic description is performed through connecting the waveforms specification of timing, simulation or measurements for modification, and then, in the next phase, the generation of the annotated HDL language structures. It is assumed, that the hardware implementation will be performed on the basis of existing CAD/CAE tools (e.g. [Xili98-99].

Control Timing Synthesis

The control timing synthesis paradigm in the mixed-mode systems is a process of the HDL code generation describing the hardware implementation for "glue" control logic for invariant or flexible (e.g. reprogrammable) analog or analog/digital parts of the mixed-mode system.

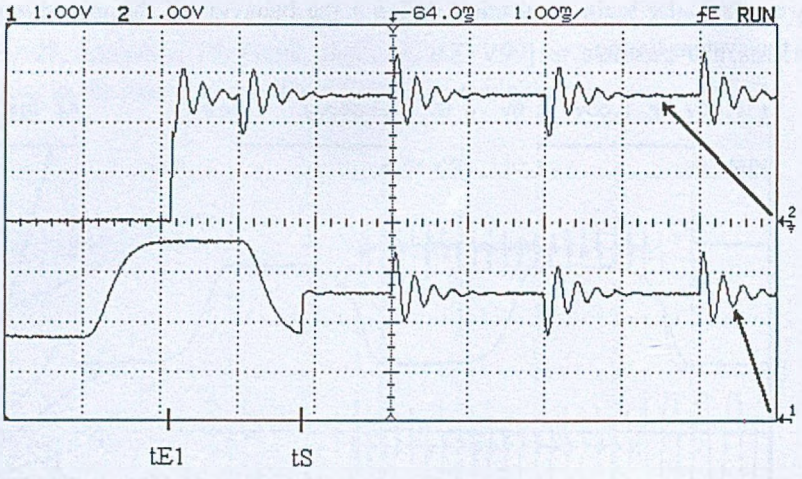


Fig. 3.43. Details of downloading transition (contd. Fig. 3.42).
Description of channels: channel 1 – system output signal, channel 2 – output of FPAA2 implementing band-pass filter.
The switching moment from the 4-th order low-pass filtering to band-pass filtering is indicated by the symbol tS (note that switching transition is hidden due to proper control timing)

Rys. 3.43. Szczegóły stanu przejściowego wpisu konfiguracji (kontynuacja rys. 3.42).
Opis kanałów: kanał 1 – sygnał wyjściowy systemu, kanał 2 – wyjście układu FPAA2 realizującego filtr środkowo-przepustowy.
Symbol tS określa chwilę przełączenia filtracji dolnoprzepustowej na filtrację środkowo-przepustową (należy zauważyć, że stan przejściowy przełączenia jest ukryty dzięki odpowiedniej sekwencji sygnałów sterujących)

The timing synthesis is composed of three fundamental phases:

Timing specification - using the Timing Editor or Timing Description Language for parameterization of signal's wave patterns.

Timing modification - the extraction of the waveforms for input/output pads in analog and analog/digital parts from the HDL description, simulation or measurements for analog and analog/digital parts of the mixed mode system and the actualization of the specified waveforms.

Code generation - the translation waveforms into the linguistic description, and in a next phase, generation of the annotated HDL language structures.

It can be stated that the control timing synthesis is performed starting from higher level of abstract description of the mixed-mode design than HDL. *The timing control synthesis*, that generates the target HDL code for timing is terminated with the *synthesis of the logic from HDL*, in order to reach the implementation of timing described in the HDL form, into the hardware.

The Case Study

We present the overview of the timing control synthesis for multielements FPAA system working as a continuous dynamic system, used in the adaptive applications [ZnPa98a, RZPV99, Znam98a], to obtain a general characterization of the problem.

Timing Specification

The FPAA can be understood as a dynamic system with configuration and parameters both set optionally on-the-fly. Those settable elements can be downloaded to the chip in a time interval not shorter then the interval of downloading. During this time the analog outputs are forced to the zero voltages. At the end of the interval of downloading, the chip starts to perform its structural function. Thus, when the FPAA has to work as a continuous dynamic system, the valid output is generated only between consecutive downloading sequences and the parallely working FPAAs are necessary. General view of the controlled FPAA chip from computer and its timing specification is presented in Fig. 3.26. We shall consider the dynamic system with an analog part of a FPAA chip described by Eqs. (3.23).

Consequently, we will consider the control timing synthesis for the dynamic system (3.23) using two FPAAs with *track/compute* capability, the analog multiplexer and an FPGA for Control logic implementation with timing specification presented in Fig. 3.26.

Timing Modification

Timing specification has to be extended upon the general control (power on state, analog, analog/digital reset states). It is important, that the internal constraints of timing have a causality nature (mainly delays). However the external constraints have to respect the features of cooperating elements of the system. In case of a system, which is considered in the following example, the timing have to fulfill a condition to "hide" the transient states of FPAA after downloading. The download of *FPAA-I (I)* starts e.g. at a moment t_1 and can not start earlier than transient state is finished (including however the Track mode) after the time t_0 finishing the *FPAA-II (I)* download. For signal *PON/RESET (Power on)* the following relation has to be fulfilled in Control logic:

$T_{PON} < T_{EN} < T_{IC}$,

where:

- T_{PON} - interval of the power on pulse *PON/RESET* width (in a case of downloading FPGA, it is *RESET* pulse),
- T_{EN} - nterval to set-up *EN (Enable)* signal for analog multiplexer equals 1, the signal *EN* can be equal 1 when the address lines of the analog multiplexer are fixed),
- T_{IC} - interval to start of downloading IC configuration to the *Part1* of the FPAA system.

Now, for analog and digital/analog parts of discussed system, we find the signal waveforms for modified Control logic timing (presented in Fig. 3.44) for analog and digital/analog parts of

discussed system. The arrows represent the signals' transition conditions. The signals' waveforms from Fig. 3.44b determine the starting point to the HDL code generation for implementation of timing control of a mixed-mode systems.

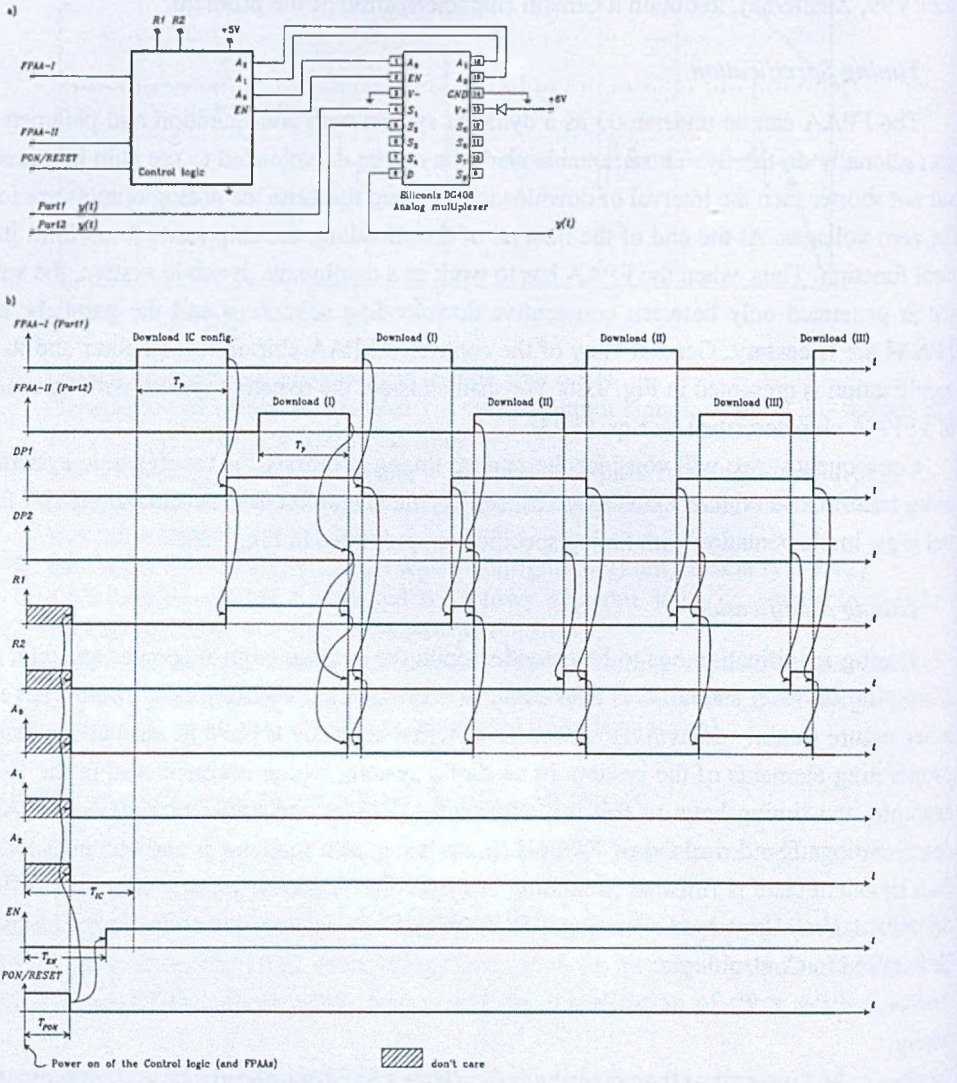


Fig. 3.44. Modified timing specification. Control logic module with analog multiplexer: a) schematic diagram, b) timing

Rys. 3.44. Zmodyfikowana specyfikacja czasowej sekwencji sterującej. Moduł układu sterowania z multiplekserem analogowym: a) schemat układu, b) czasowa sekwencja sterująca

Concluding; considering the states, modes, types of variables, intervals, parameters and signals' transition conditions in a modified timing specification of a mixed-mode system tim-

ing, the TDL (Timing Description Language) can be defined for a timing specification description.

Compiler

The logical structure of a software system translating the source code in the TDL language into target HDL code (VHDL or Verilog) is presented in Fig. 3.45.

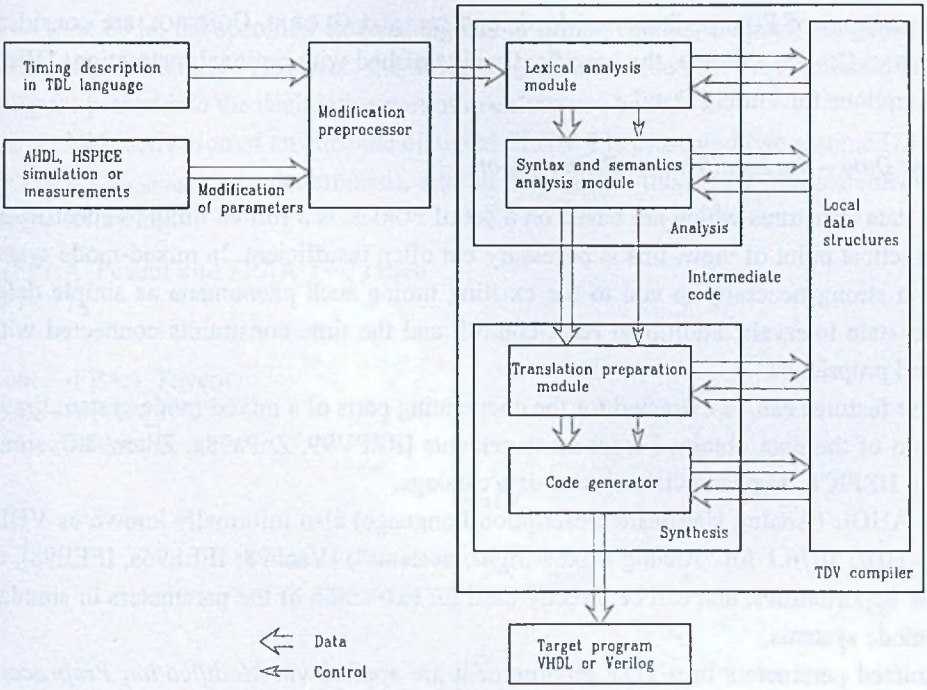


Fig. 3.45. Logical structure of a system processing the source code (TDL language) into target code VHDL (or Verilog)

Rys. 3.45. Struktura logiczna systemu przetwarzania kodu źródłowego opisu (język TDL) do kodu wynikowego w VHDL'u (lub Verilog'u)

The structure of a TDV (Timing Description to Vhdl or verilog) compiler is classical [AhSU86] however, the following should be noted. When the code generation takes place in the *Synthesis* module of a compiler, only the synthesizable structures (ref. to p. *Constraints in TDV*) of the HDL language are implemented.

Input Data – the Language

As far as mixed-mode systems' applications are considered, we may assume that a designer of a mixed-mode system must not be an ASIC specialist. Even more, growing development of reprogrammable circuits, microsensors, micromachines [ESCI99, MIXD01], and

microreactors [PVHZ01] stimulates the expansion of mixed-mode systems from electronics through electromechanics to chemistry and biology.

It has been assumed so, that a user is capable to describe the timing in descriptive form declaring signals, their parameters and inter-signals causality dependencies. In this manner it was possible to hide the formalism of a HDL language to the user. The sentences of TDL language present limited set of sentence patterns FORMs which have to be parameterized by user. The consistency of declaring data is checked by the *Analysis* module of TDV compiler. Actually, three types of FORMs: SIGNAL, MODIFICATION, and GLOBAL CONTROL are considered. For GLOBAL CONTROL FORM, the specification is finished with optional instruction: "Visualize assumptions for Timing Data".

Input Data – the Modification Preprocessor

The data structures which are based on a set of FORMs, is a formal timing's specification. From practical point of view, this is necessary but often insufficient. In mixed-mode systems there is a strong necessity to add to the existing timing such phenomena as simple delays, transient state intervals, additional reset control, and the time constraints connected with a download proprieties.

These features can be extracted for the cooperating parts of a mixed-mode system through utilization of the data obtained from measurements [RZPV99, ZnPa98a, Znam98a], simulation (e.g. HSPICE, logic simulators), and data catalogs.

The AHDL (Analog Hardware Description Language) also informally known as VHDL-AMS (VHDL 1076.1 for "Analog Mixed-Signal systems") [Vach98; IEEE96a, IEEE98], creates new opportunities, and can be directly used for extraction of the parameters in simulated mixed-mode systems.

Extracted parameters in a TDV environment are applied via *Modification Preprocessor* (Fig. 3.45) and in a FORM named MODIFICATION finalizing the modified timing specification.

Processing in TDV

After modification (if any) for declared set of FORMs, the local data structures are generated, and mapped in *Synthesis* module of TDV to the selected set of HDL statements.

Basic statements of VHDL used in mapping constitute a **process** (syntax according with [IEEE94, IEEE96b] statement:

```
process_statement::=
    [process_label:]
        process (sensitivity_list)[is]
            process_declarative_part
        begin
            process_statement_part
        end process [process_label];
```

and a **if ... then** statement:

```
if_statement::=
    [if_label:]
            if condition then
                sequence_of_statements
            {elsif condition then
                sequence_of_statements}
            [else   sequence_of_statements]
            end if [if_label];
```

In a target code, the specified external signals in timing (inputs, outputs) are gathered as ports of **entity** declaration. However, the declared (and introduced by TDV) internal signals of timing are placed into the declarative part of **architecture** body.

In Fig. 3.46, activation of an attribute of signal FPAA_I is presented (we assume DP1 signal for $t \leq t_{\text{moment of event}}$ is undetermined), and an outcome of this event in a statement **if ... then** is the following:

```
if (FPAA_I'event and FPAA_I='0') then
DP1<='1';
```

thus

```
event →FPAA_I'event
result →FPAA_I='0'
then → DP1<='1'.
```

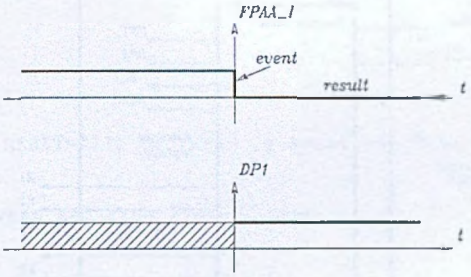


Fig. 3.46. The attribute 'event for an exemplary signal FPAA_I
Rys. 3.46. Atrybut 'event przykładowego sygnału FPAA_I

A **process** P_A0 from listing fpaa.VHD (see below the code describing ASIC, implementing the timing) is an example of expression of the SIGNAL FORM for a timing signal A_0 into the VHDL code:

```
P_A0: process(RESET,R1_1,R2_2)  begin
if (RESET'event and RESET='0') or (R2_2'event
and R2_2='0') then A0<='0';
elsif (R1_1'event and R1_1='0')    then A0<='1'; end if;
end process P_A0;
```

The signals R1_1 and R2_2 (copies of R1 and R2) had to be introduced during a code generation, since the R1 and R2 are ports, and can not be on a sensitivity list of a **process** statement.

Constraints in TDV

It is assumed that the HDL code implemented to hardware, uses existing CAD/CAE tools.

The limitations of the structures of HDL take form of: "wait for X ns" and " ... after XX ns" in case of VHDL, and "#XX" and "assign #XX ... " in case of Verilog.

Those HDL structures do not synthesize to a component, they are not supported by the well known automatic synthesis tools, because of lack of accurately determined (depended on implementation) results of a performed synthesis [Skah97, Xili99].

On the other hand, those structures are indispensable to delay specification, so in the TDV they are replaced with the parameterized VHDL counter's code.

Example – FPAA/FPGA Application

The block diagram of a modified timing specification from Fig. 3.44 in form of entity declaration and a corresponding architecture body of VHDL language for ASIC/FPGA, is presented in Fig. 3.47.

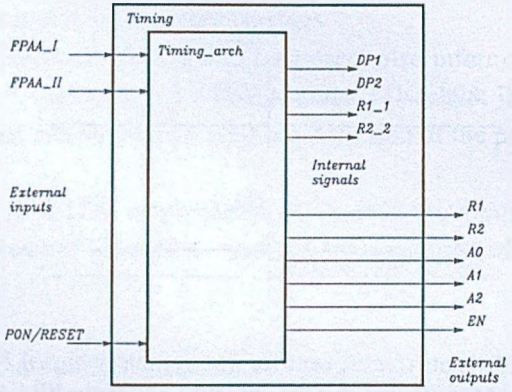


Fig. 3.47. Timing entity and Timing_arch architecture of the timing Control logic in the mixed-mode system

Rys. 3.47. Struktura entity Timing oraz architektura Timing_arch układu czasowej sekwencji sterującej systemu mixed-mode

The VHDL code for ASIC/FPGA from Fig. 3.47 (the code for a counter implementing 300ms delay in EN signal is not included), takes the form:

```
--
--
-- File: c:\my designs\fpaa\SRC\fpaa.VHD
```

```
--

library IEEE;
use IEEE.std_logic_1164.all;

entity Timing is
   port (
      FPAA_I : in STD_LOGIC :='0';
      FPAA_II: in STD_LOGIC;
      RESET  : in STD_LOGIC;
      R1: out STD_LOGIC :='U';
      R2: out STD_LOGIC :='U';
      A0: out STD_LOGIC :='U';
      A1: out STD_LOGIC :='U';
      A2: out STD_LOGIC :='U';
      EN: out STD_LOGIC :='0'
   );
   end Timing;

   architecture Timing_arch of Timing is
   signal DP1: STD_LOGIC :='0';
   signal DP2: STD_LOGIC :='0';
   signal    R1_1: STD_LOGIC :='U';
   signal R2_2: STD_LOGIC :='U';
   begin

   P_DP1: process(FPAA_I)
   begin
   if (FPAA_I='0' and RESET='1') or (FPAA_I'event and FPAA_I='1')
      then
      DP1<='0';
      elsif (FPAA_I'event and FPAA_I='0') then
      DP1<='1';
   end if;
   end process P_DP1;

   P_DP2: process(FPAA_II)
   begin
   if (FPAA_II='0' and RESET='1') or (FPAA_II'event and FPAA_II='1')
      then
      DP2<='0';
      elsif (FPAA_II'event and FPAA_II='0') then
      DP2<='1';
   end if;
   end process P_DP2;

   P_R1_1: process(RESET,DP1,DP2)
   begin
   if (RESET'event and RESET='0') or (DP2'event and DP2='1')
      or (DP2'event and DP2='0')
      then
      R1_1<='0';
      R1<='0';
      elsif (DP1'event and DP1='1')then
      R1_1<='1';
      R1<='1';
   end if;
   end process P_R1_1;

   P_R2_2: process(RESET,DP2,DP1)
   begin
   if (RESET'event and RESET='0') or (DP1'event and DP1='0')
      then
      R2_2<='0';
```

```
      R2<='0';
   elsif (DP2'event and DP2='1') then
      R2_2<='1';
      R2<='1';
   end if;
   end process P_R2_2;

   P_A0: process(RESET,R1_1,R2_2)
   begin
   if (RESET'event and RESET='0') or (R2_2'event and R2_2='0')
      then
      A0<='0';
   elsif (R1_1'event and R1_1='0')
      then
      A0<='1';
   end if;
   end process P_A0;

   P_A1: process(RESET)
   begin
   if (RESET'event and RESET='0') then
      A1<='0';
   end if;
   end process P_A1;

   P_A2: process(RESET)
   begin
   if (RESET'event and RESET='0') then
      A2<='0';
   end if;
   end process P_A2;

   P_EN: process(RESET)
   begin
   if (RESET'event and RESET='0') then
      EN<= '1' after 300 ms;
   end if;
   end process P_EN;

end Timing_arch;
```

The results of simulation [Alde98] of the VHDL (fpaa.VHD) code implementing the timing control of FPAA/FPGA mixed-mode system, are presented in Fig. 3.48.

It is interesting to evaluate the time delays of a logic gates of ASIC/FPGA through implementation of the timing from Fig. 3.48. The experiments were performed to measure the time delay in an AND gate implemented in Xilinx XC 4003E chip from AND VHDL code (using process statement and not a Xilinx' library AND gate). The results of simulation based on implementation by Xilinx (XC4003E) showed that the gate delay is approximately 8ns. However, considering the FPAA download time from SRAM memory, which is of order of 30ms this delay is negligible and the speed of FPGA's timing implementation quite is sufficient.

3.6.7. Concluding Remarks

The experiments were performed to optimize the reconfiguration process in applications of plant simulation in predictive control, and adaptive control. In case of plant simulation in

predictive control, we validated the behavior of the two FPAAs and multiplexer system modeling the dynamic plant in the speeded up time scale. Experiments and validation of simulated plant were performed from *initial conditions* mode in first FPAA, *compute* mode in first FPAA (with parallely tracking by second FPAA) through start of downloading in first FPAA with parallel start to compute in second FPAA. The FPAA configurations consecutively downloaded, assure coping of the state vector in the plant model (which is changing with time). Non-critical transient state in *track* mode is better then 15μs. Transient state in switching the output signals in FPAA and multiplexer in not longer than 2μs. Imperfection of copying state variable reaches value approximately 1.5%. These imperfection can be easily improved by tuning the switches, multiplexer and control signal (start of download) operation.

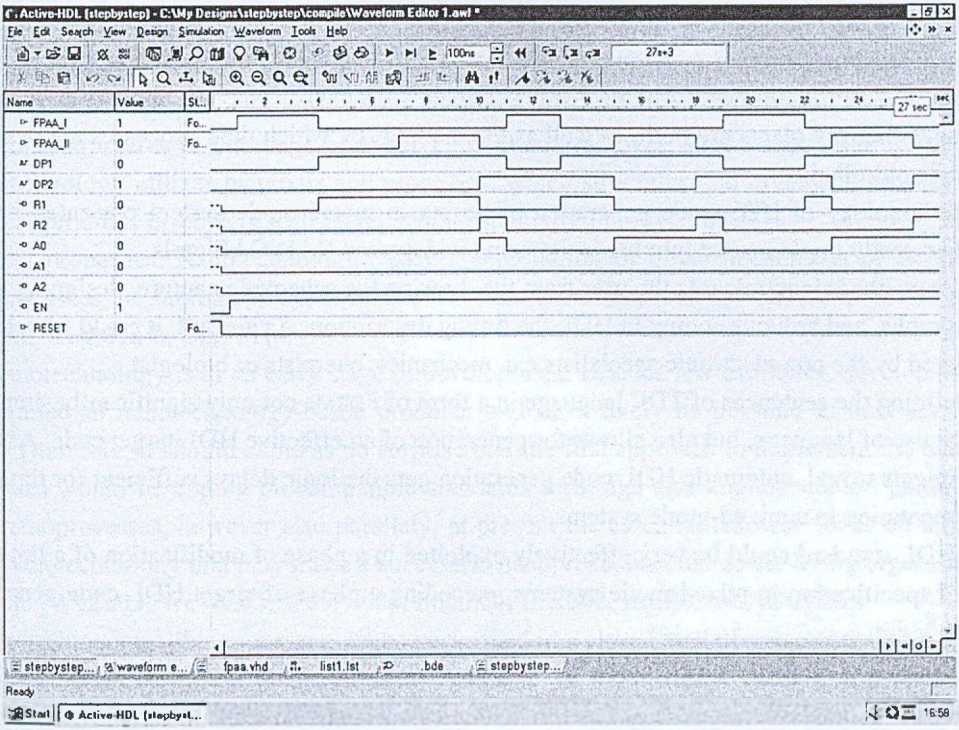


Fig. 3.48. Timing simulation results for VHDL code (file fpaa.VHD)
Rys. 3.48. Wyniki symulacji czasowej sekwencji sterującej w układzie sterowania opisanym kodem VHDL (plik fpaa.VHD)

In case of FPAA system used in adaptive control the goal of measurements was calculation of the time of downloading of implemented reconfigurable controller with alternative transfer functions in AN10E chips and determination of the interval time "hiding" the dynamic imperfections during on-the-fly changes in the modes of FPAAs.

The experiments showed that the transfer function can be changed approximately 30 times per second. The transient state after download process is not longer than 2ms for applied transfer functions realizing this adaptive controller.

The validation of multi-chip, reconfigurable FPAA systems used in applications of plant simulation in predictive and adaptive control, however, the modeling results are general and can be used in constructing systems that support dynamically reconfigurable analog/digital hardware. The time delay for an FPAA application is determined by proper parameters, such as download time and transient states in the interval of switching of CAB. The FPGA provides the parameters for the reconfigured function and takes the appropriate time delay out of the table. Such an adaptive solution provides for a variety of different adaptive applications with fast switching behavior. For example, development of chemical microreactors and micromixers is rapidly progressing due to factors such as elimination of scale-up procedures, higher precision of mixing and component contact surfaces, and minimization of processing hazards. Field Programmable Analog Arrays coupled with microreactor technology promises to change the way plants are built, as well as the methods by which their processes are designed and controlled.

Methodology of HDL code generation of timing in mixed-mode system presented here could be easily implemented into hardware using widespread CAD/CAE tools.

This methodology releases the user from the drawing the schematic capture, designing the FSM graphs, and arduous coding in HDL the timing description. As a result, it could be easily employed by the non-electronic specialists e.g. mechanics, chemists or biologist.

Defining the sentences of TDL language in a form of FORMS not only significantly simplifies the use of language, but also allows for generation of an effective HDL target code. As an experiments reveal, automatic HDL code generation gets the logic delays sufficient for timing implementation in a mixed-mode systems.

AHDL standard could be very effectively exploited in a phase of modification of a timing control specification in mixed-mode systems, preceding a phase of target HDL code generation.

4. SWITCHING IN THE NANOSTRUCTURES

The essence of new technologies called nanotechnologies is the capability to work at the molecular level in order to build a large molecular structures with new, desirable aggregation and properties. Compared to the features of single molecules of about 0.5nm, behavior of molecular structures in the range of about 1 to 100nm and over, shows significant changes. Nanotechnology utilizes materials and processes, which structures and organization leads to the final products or objects with novel and substantially improved biological, chemical, and physical properties. Nanotechnologies enable exploitation of novel phenomena or existing nanoprocesses in biological systems due to their nanoscale size [WKZW04, WeWZ04, Roco02, Wegr01a-b, Drex81].

Nanotechnology is in an early stage of development. Besides few examples, development of commercial nanotechnology-based products will most likely be possible in next several years. Therefore, it should come as no surprise that the first approach to implement the nanoprocesses would be coping biocompatible standards in design and implementation phase of such nanoprocesses, however also parallely, at present the essential research focus on molecular nanotechnology that may make a successful nanoprocesses outside the living organisms, possible [WeZn03, WeWZ02, WeWZ03a, Znam04, IEEE02, IEEE03a-b, ICCE03].

Those biocompatible processes can be performed in a closed area of space containing proper quantities of substrates (basic elements) and a set of molecules working in a predefined manner determined by their chemical construction, including changes of chemical activity reached usually by the conformational changes. These molecules play a role of a control system, which is stimulated by external signal molecules (and of course performing homeostatic functions) coming from outside of the closed area of space to its surface, fulfilling the function of nanoprocess border. The molecular control system performs its control tasks in fixed cycles of transformations called signal cascades. We shall call this kind of system performing nanoprocess – a nanonetwork. In determined conditions, the selected substrates (inorganic ions and most of metabolites e.g. sugars, amino acids, and nucleotides) and final products can penetrate through the border of the process. Excluding selected ions fulfilling the control functions in the signal cascades, the external stimulating signal molecules only activate the

receptors placed in the border of a nanonetwork. The process of internal transformations and conversions of control molecules in signal cascades expressed as a control of nanoprocesses in a nanonetwork, is called a signal transduction [Znam03a].

Generally, those processes of internal transformations and conversions of control molecules are called conformations modifications or simply conformation switching because of high-speed of changes. The conformation switching of control molecules in the complexes of signal transduction cascades we will call signaling switching.

In this chapter, basing on simulation approach, we will consider the problem of conformation switching in nanostructures and we'll propose the hierarchical description of signaling switching in the nanonetworks.

4.1. Description of Nanostructures

4.1.1. Data Formats

File Format PDB (Protein Data Bank)

The Protein Data Bank is a computer-based archival database for macromolecular structures. The database was established in 1971 by Brookhaven National Laboratory, Upton, New York. In 1999 the Protein Data Bank moved to the Research Collaboratory for Structural Bioinformatics (Rutgers University, San Diego Supercomputer Center at University of California, San Diego, and National Institute of Standards and Technology) [BWFG00]. In the beginning the archive had held seven structures, in 2000 contained approximately 10500 structures, however, the administrators of the Data Bank estimate that the tremendous influx of data soon to be fueled by the post genome-sequencing era, the number of structures could triple and even quadruple in size in 2005. In the Protein Data Bank, entries represent the structure of a single molecule, or that of a macromolecular complex e.g. a protein-protein or protein-DNA complexes. In the other, generally, biological databases, information can be organized in a different manner. In the EMBL and GenBank/NCBI-Entrez-Nucleotide databases it is one entry per gene [BBCH00, BBLO99, NCBI03], in SWISS-PROT or NCBI-Entrez-Protein there are the sequential description of an individual polypeptide [BaAp00, NCBI03]. The primary focus of the standardization of molecule structure description in the Protein Data Bank was the readable (in ASCII) formatted text file, containing the 3-dimensional coordinates in angstroms description of spatial position of atoms in a molecule. The short PDB format description is provided in Appendix IV, however, the complete PDB file specification can be found in PDB documentation [CCDE96].

The biological databases including Protein Data Bank were created chiefly for storing data on primary, secondary, tertiary, and quaternary structure of proteins, however in parallel, meaning efforts have also be made to include into databases information about biological function of the stored data on the molecules. It is possible to consider the traditional databases

as a distributed basis for specialized databases [HNME00] capable to process data from new experimental procedures for large scale functional characterization of gene products such as microarray based gene expression analysis [BrBo99, DeIB97] or the techniques for analyzing expressed proteins (the proteome) [Will99].

File Format mmCIF (Macromolecular Crystallographic Information File)

The mmCIF was developed in 1990 by the IUCr Commission on Crystallographic Data and IUCr Commission on Journals [Nucl01b]. This is essentially a dictionary of information describing a chemical structure in broad sense e.g. internal geometry, average values for the bonds, angles and torsions in the structure, polarizability and hydrophobicity, the mmCIF also contains the adequate information about the macromolecular crystallographic experiment and its results as well.

The tools that currently exist include:

CIFLIB	– C Language Application Program Interface
cif2pdb	– format translator from mmCIF format to PDB
pdb2cif	– translator from PDB format to mmCIF
CIFPARSE	– a function library to provide convenient and efficient access to mmCIF data files and others.

The selected PDB files describing the structures of the molecules discussed in this chapter, are presented in Appendix IV.

4.1.2. Graphics

RasMol – a Molecular Graphics Program

The graphic program RasMol [Sayl01] includes spacefilling spheres, sticks, wireframes, ball and stick, atom labels, solid and strand biomolecular ribbons molecules presentation. The RasMol approves the input formats PDB, mmCIF and a few others.

PDB and RasMol Implementation (Example)

Below, the description (part of the file 208d.pdb [Nucl01a]) in PDB format of selected nucleic acid molecule is presented. The result of loading this information in RasMol program is reflected in Fig. 4.1 in the stick representation of molecule.

```
HEADER    DEOXYRIBONUCLEIC ACID                    26-APR-95   208D      208D   2
COMPND    DNA (5'-D(*GP*CP*GP*AP*AP*TP*TP*CP*G)-3')                      208D   3
SOURCE    SYNTHETIC                                                      208D   4
EXPDTA    X-RAY DIFFRACTION                                              208D   5
AUTHOR    L.VAN MEERVELT,D.VLIEGHE,A.DAUTANT,B.GALLOIS,G.PRECIGOUX,      208D   6
AUTHOR   2 O.KENNARD                                                     208D   7
REVDAT    1   15-SEP-95 208D    0                                        208D   8
JRNL        AUTH   L.VAN MEERVELT,D.VLIEGHE,A.DAUTANT,B.GALLOIS,         208D   9
JRNL        AUTH 2 G.PRECIGOUX,O.KENNARD                                 208D  10
JRNL        TITL   HIGH-RESOLUTION STRUCTURE OF A DNA HELIX FORMING      208D  11
JRNL        TITL 2 (C(DOT)G)G BASE TRIPLETS                              208D  12
JRNL        REF    NATURE                    V. 374   742 1995          208D  13
JRNL        REFN   ASTM NATUAS  UK ISSN 0028-0836                 0006  208D  14
....
```

```
....
ATOM      1  O5*   G A   1       6.009   7.501 -13.738  1.00 20.11       208D  89
ATOM      2  C5*   G A   1       5.971   8.717 -14.473  1.00 18.89       208D  90
....
....
ATOM    360  C5    G B   9       7.836  20.923 -11.167  1.00 12.96       208D 448
ATOM    361  C6    G B   9       7.838  19.508 -11.113  1.00 12.33       208D 449
ATOM    362  O6    G B   9       6.897  18.731 -11.169  1.00 11.58       208D 450
ATOM    363  N1    G B   9       9.109  19.014 -11.044  1.00 12.17       208D 451
....
....
HETATM  455  O   HOH     96       5.791  10.465  -8.008  1.00 43.42       208D 543
HETATM  456  O   HOH     97       8.563  11.974  -7.756  1.00 56.28       208D 544
MASTER        61    0    2    0    0    0    0    6  454    2    0    2  208D 545
END                                                                      208D 546
```

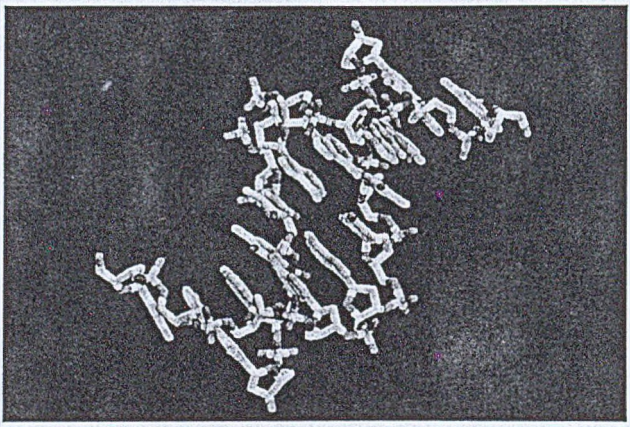


Fig. 4.1. Stick representation of molecule. User-set angles. Zoom equals to 150. Molecule DNA

Rys. 4.1. Reprezentacja belkowa molekuł. Kąty obserwacji ustawione przez użytkownika. Zoom 150. Molekuła DNA

4.1.3. Nanostructures Synthesis – Protein Translation Process

Proteins, the working nanostrucrures in a biological organisms, express the programs of organism's architecture and activity encoded by genes. The remarkable range of their activity is presented in their functions of enzymatic catalysis, functions of transporting and storage, effective motion and mechanical support, immune protection, control of the processes of growth and differentiation.

The basic molecules carrying an information in signal transduction cascades of biological nanonetworks are proteins also, what is more, the same protein may carry diverse information through its conformation switching. These phenomena take place in a form of post-translational modifications or, as an appropriate stimuli results.

As an illustration, we will briefly discuss the signal cascades in the process of translation control [Cell03] (signal cascades in a differently graphic convention are presented in Figs. 4.22 and 4.23), which can be used for selected proteins production (Fig. 4.2).

The mechanism of protein synthesis is a process called translation, because a string of letters of the four-letter alphabet of nucleic acids accordingly with genetic code is translated into string of amino acids of the 20-amino acid alphabet, forming proteins. The process takes place in a ribosome structure (complex of subunits 40S and 60S rRNA) in presence of at least one kind of tRNA and activating enzyme for each amino acid. The translation process is performed in a ribosome moving along the mRNA chain. Protein synthesis takes place in initiation, elongation, and termination stages.

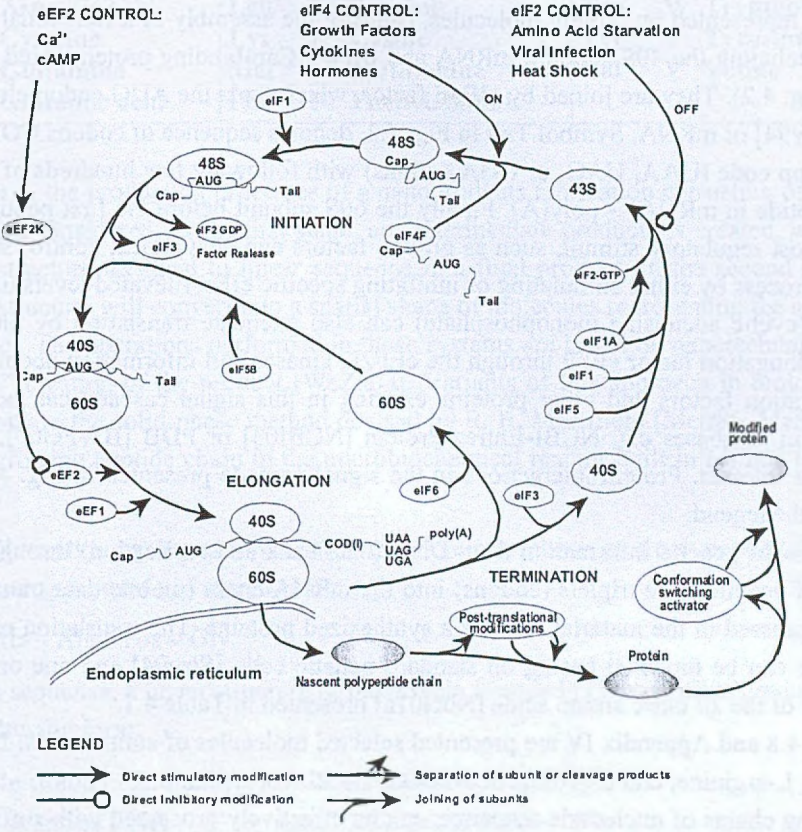


Fig. 4.2. The signal cascade in a nanonetwork (translation control)
Rys. 4.2. Kaskada sygnałowa w nanosieci (sterowanie translacją)

The *initiation stage* results in connecting of the initiator tRNA to the start signal in mRNA. The *termination stage* takes place when a stop signal in the mRNA is read by the protein release factor. Each nucleotide triplet, or codon, in mRNA chain encodes a specific amino acid. In the *elongation stage*, each molecule of tRNA binds only the amino acid proper to a particular codon, and tRNA recognize a codon by means of a complementary nucleotide sequence named anticodon. The movement of RNA in relation to the ribosome to the next

codon is powered by the hydrolysis of GTP. Consecutive codons (translation direction is from 5' to 3' end of mRNA) interact with proper transferred amino acid molecules and the peptide chain shoves up forming the protein. When the termination stage occurs, a completed protein is released from the ribosome [Stry94, LBZM01, GrNo97]. Next, the processes of modifications after translation take place [ZnZu02b, WeWZ02].

Synthesis of a new protein is highly controlled process (Fig. 4.2) that allows rapid cellular responses to diverse stimuli [Cell03, Rhoa99]. Initiation of protein synthesis begins after a separation of the ribosome into its 40S and 60S subunits. Different eukaryotic initiation factors (eIFs) represented by protein molecules, catalyze the assembly of a functional ribosomal complex including the 40S subunit, mRNA and tRNA. Cap-binding proteins bind the cap of mRNA (Fig. 4.2). They are joined by eIF4F factor, which finds the AUG codon closest to the 5' end [Stry94] of mRNA. Symbol Tail in Fig. 4.2, denotes sequence of codons COD(i) ended with the stop code (UAA, UAG, or UGA codons) with following few hundreds of A (adenosine nucleotide in mRNA) – poly(A). Finally the 60S subunit before the first peptide bond is formed. Most regulatory stimuli, such as growth factors and heat shock, control steps of the initiation process by either stimulating or inhibiting specific eIFs. Elevated levels of Ca^{2+} ions or cAMP (cyclic adenosine monophosphate) can also attenuate translation by blocking the action of elongation factor eEF2 through the eEF2K kinase. Full information about the initiation, elongation factors and other proteins existing in this signal cascade can be extracted from protein databases e.g. NCBI-Entrez-Protein [NCBI03] or PDB [BWFG00], reachable through the Internet. Protein interactions in the signal cascade presented in Fig. 4.2, are explained in the legend.

The flow of genetic information from DNA (data bank and replication) through the transcription of genetic code triplets (codons) into the mRNA chain (mobile data transmitter) finally is expressed in the material form as a synthesized proteins. The translation process in a static sense can be modeled basing on standard genetic code [Stry94] and one or two letter description of the 20 basic amino acids [Nucl01a] presented in Table 4.1.

In Fig. 4.8 and Appendix IV are presented selected molecules of amino acids: L-histidine, L-cysteine, L-arginine, and L-proline in different visual representations.

The long chains of nucleotide sequence, can be effectively processed with sufficient software with many parameters [ExPA01], and next processed [Pond01] into PDB files for consecutive computations. Visualization can be effectively performed e.g. with the RasMol program [Sayl01] or the other molecular graphics tools [MaKr04].

The conformation (and the functional biological properties) of the protein molecule depends not only on the sequence of amino acids but also on the torsion angles of peptide bonds in the peptide chain. These processes are realized in the phase of so called post-translational modifications or for folded proteins, through the conformations switching of the signaling proteins participating in the signal cascades of the signal transduction paths. In self-replication processes [Wegr01a-b, WeWZ02] such as a self-replication cycle of a living cell, the

proper switching of post-translational conformations of signaling proteins [Znam03a] plays a crucial role in a cell's proliferation process as well as in either keeping it alive or making it die.

Table 4.1

Symbols for amino acids

Ala	A	Alanine	Gly	G	Glycine	Pro	P	Proline
Arg	R	Arginine	His	H	Histidine	Ser	S	Serine
Asn	N	Asparagine	Ile	I	Isoleucine	Thr	T	Threonine
Asp	D	Aspartic acid	Leu	L	Leucine	Trp	W	Tryptophan
Cys	C	Cysteine	Lys	K	Lysine	Tyr	Y	Tyrosine
Gln	Q	Glutamine	Met	M	Methionine	Val	V	Valine
Glu	E	Glutamic acid	Phe	F	Phenylalanine			

In general, the production processes of a nanoproducts fabrication consisting of two main stages can be considered. In the first stage, an "intermediate product" is created, with linear, molecular structure identical to linear sequence in a final product. In the second stage, that flat, linear structure will convert into a spatial shape of molecules representing the appropriate final product. The operations performed in those systems are based on nanotechnologies or a "bottom-up" creation of the product [WeZn03]. Variants of this approach in biological product creation are the solid-phase method devised by R. B. Merrifield [Merr86, McMu00] and forming a growing peptide chain in the microbiochemical reactor built in MEMS technology [HFNS97].

As an illustration we assume [WeZn03] the protein synthesis as a polypeptide determined by the following sequence of amino acids:

Met – Ala – Ala – His – Gly

For this sequence, a linear structure of the protein is coded in DNA helix (product code 15 bp) in a following form:

Template strand of DNA 3' – TACCGTCGTGTGCCT – 5'
Coding strand of DNA 5' – ATGGCAGCACACGGA – 3'

Basing on RasMol program the graphic visualization of this fragment of DNA is presented in Fig. 4.3.

As a result of transcription, the mRNA strand is created as a complementary to its DNA template (the RNA has the same base-sequence as the coding strand of DNA except for uracil in place of thymine) getting the following form:

Strand of mRNA 5' – AUGGCAGCACACGGA – 3'

The RNA helix, which establishes the "gluey matrix" in synthesis process [WeZn03] is presented in Fig. 4.4.

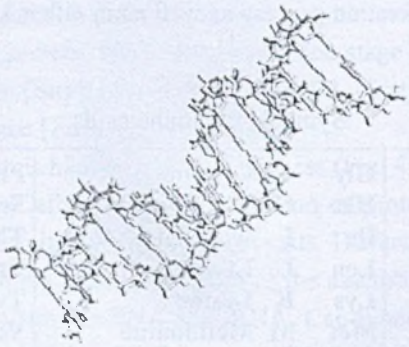


Fig. 4.3. The protein code (DNA coding the linear structure of the considered protein)
Rys. 4.3. Kod proteiny (fragment DNA kodujący liniową strukturę rozważanego białka)

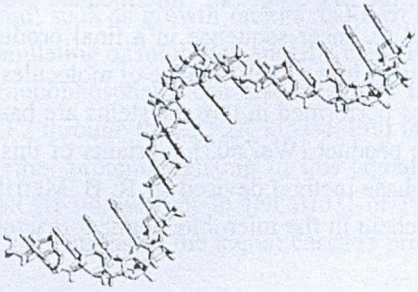


Fig. 4.4. RNA polymer establishing a "gluey matrix" for protein synthesis
Rys. 4.4. Polimer RNA stanowiący „lepką matrycę" dla syntezy białka

This matrix determines the sequence of synthesized amino acids presented in Fig. 4.5.

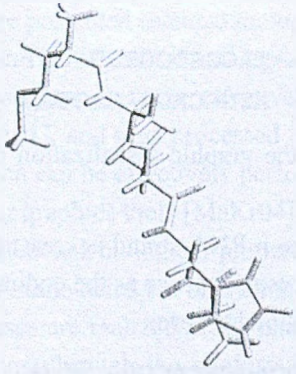


Fig. 4.5. Intermediate pentapeptide
Rys. 4.5. Pośrednia forma pentapeptydu

An illustration of the post-translational modification of the considered pentapeptide performed for alanine torsion angles is presented in Fig. 4.6.

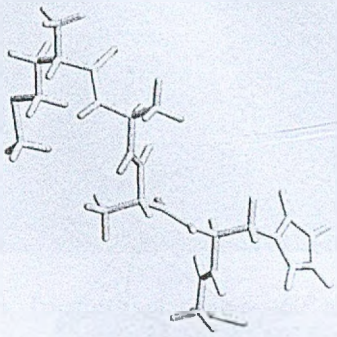


Fig. 4.6. Intermediate pentapeptide modification
Rys. 4.6. Modyfikacja pośredniej formy pentapeptydu

4.2. Conformation Modifications

4.2.1. Polypeptide Structure

The three-dimensional structure of a polypeptide can be completely described by placing it in a Cartesian coordinate system and listing *x, y, z* coordinates for each atom in the chain. However, when we simulate the modification processes, the synthesis programs generating the conformation of the main chain of polypeptide use the amino acids library and need the information on the angles between α-carbons bonded with their side chains and a contiguous peptide groups [Znam02]. The backbone of a chain of amino-acid residues determined by set of torsion angles, is presented in Fig. 4.7.

The backbone conformation of an amino-acid residues can be specified by listing the torsion angles φ (rotation around the nitrogen-α-carbon bond in the main chain), and ψ (rotation around the α-carbon-carbon bond in the main chain of the polypeptide). The relationship between the peptide groups, α-carbons and torsion angles can be expressed in a following form:

$$\rightarrow \mathrm{PB} \rightarrow \phi_1 \rightarrow \mathrm{C}_{\alpha 1} \rightarrow \psi_1 \rightarrow \mathrm{PB} \rightarrow \phi_2 \rightarrow \mathrm{C}_{\alpha 2} \rightarrow \psi_2 \rightarrow \mathrm{PB} \rightarrow \tag{4.1}$$

where PB denotes the peptide bond and $\mathrm{C}_{\alpha i}$ is the *i*-th α-carbon atom.

The zero for torsion angle φ is defined with the N—H bond trans [Lieb92] to the C_α—C' bond, and the zero position for ψ is defined with the C_α—N trans to the C=O bond. The peptide-bond torsion angle ω is generally 180°, this is with C=O bond trans to the N—H bond [Lieb92] and the sets of χ angles for the side chains, in approximation are assumed to be stiff.

The torsion angles play a crucial role in the conformation of proteins because the three-dimensional structure of protein determines its biological functions. On the other hand not all

combinations of torsion angles are possible, as many leads to collision between atoms in adjacent residues. The possible combinations of φ and ψ angles that do not lead to collision can be plotted on a Ramachandran map [RaSa68, HoZO02].

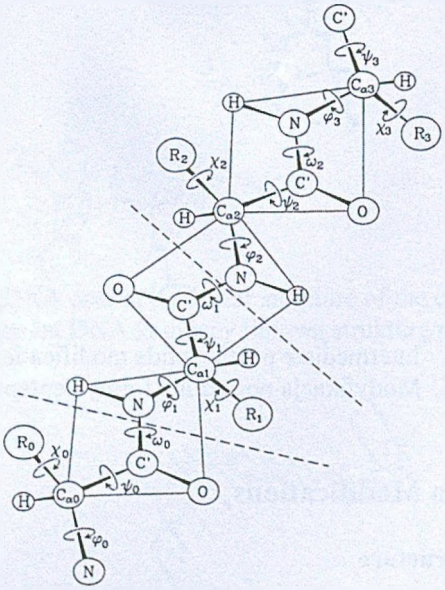


Fig. 4.7. Definition of protein torsion angles φ, ψ, ω and χ in the polypeptide sequence. The limits of a residue #1 are indicated by dashed lines, the chain is shown in a fully extended conformation ($\varphi_1=\psi_1=\omega_1=180^\circ$) [Lieb92]

Rys. 4.7. Definicja kątów torsyjnych φ, ψ, ω and χ w sekwencji polipeptydu. Linie przerywane oznaczają granice reszty aminokwasowej (#1), a łańcuch przedstawiono w formie rozciągniętej ($\varphi_1=\psi_1=\omega_1=180^\circ$) [Lieb92]

It can be simply observed that the small changes of the torsion angles cause fundamental changes in conformation of the polypeptide in a case, when the chain of amino acids is very long. In the dipeptide with amino acid [ZnZu02a, Znam02, Klot01] sequence His-Cys presented in Figs. 4.8 and 4.9. where the torsion angles φ and ψ have a different values.

The long chains of amino acids or nucleotide sequence, can be effectively processed basing on the molecular modeling software and converted [Pond01] into PDB files for consecutive computations [Znam01b, ZnZu02a, WeWZ02].

We will present the model of translation process when the peptide chain is synthesize as a straight protein and a next one, when the torsion of selected peptide bonds takes place. The initiating methionine is removed. Let we consider the mRNA nucleotide chain coding the epidermal growth factor (EGF) [Stry94]:

AAU AGC UAU CCU GGU UGU CCU AGU AGU UAU GAU GGU UAU UGU UUA AAU GGU GGU GUA UGU AUG CAU AUA GAA AGU UUA GAU AGU UAU ACA UGU AAU UGU GUA AUA GGU UAU AGU GGU GAU AGA UGU CAA ACA AGA GAU UUA GAU GG UGG GAA UUA AGA

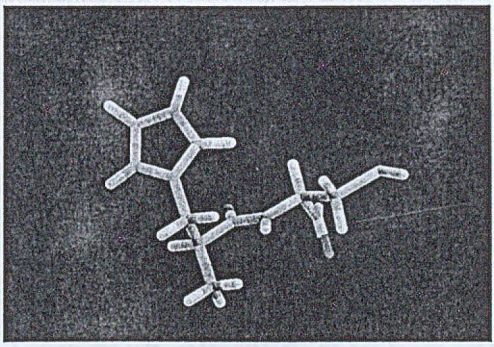
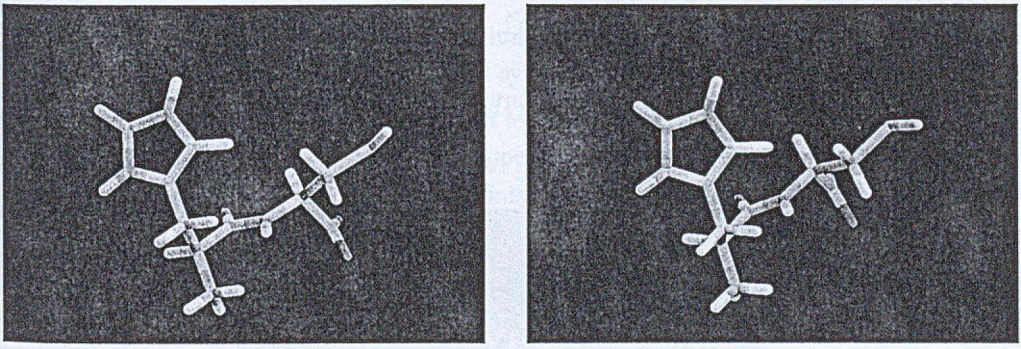


Fig. 4.8. Dipeptide His-Cys. Torsion angles $\varphi_{His} = -60^{\circ}$ and $\psi_{His} = -60^{\circ}$ for histidine molecule, and $\varphi_{Cys} = -60^{\circ}$ and $\psi_{Cys} = -60^{\circ}$ for cysteine. Stick representation of molecule [Sayl01]

Rys. 4.8. Dipeptyd His-Cys. Kąty torsyjne dla histydyny wynoszą $\varphi_{His} = -60^{\circ}$ oraz $\psi_{His} = -60^{\circ}$, natomiast dla molekuły cysteiny $\varphi_{Cys} = -60^{\circ}$ i $\psi_{Cys} = -60^{\circ}$. Reprezentacja belkowa molekuł [Sayl01]



a) b)

Fig. 4.9. Dipeptide His-Cys, a) the torsion angles $\varphi_{His} = \psi_{His} = -60^{\circ}$ for histidine, and $\varphi_{Cys} = -90^{\circ}$ and $\psi_{Cys} = -60^{\circ}$ for cysteine, b) $\varphi_{His} = -60^{\circ}$ and $\psi_{His} = -85^{\circ}$ for histidine and $\varphi_{Cys} = \psi_{Cys} = -60^{\circ}$ for cysteine

Rys. 4.9. Dipeptyd His-Cys, a) kąty torsyjne $\varphi_{His} = \psi_{His} = -60^{\circ}$ dla histydyny oraz $\varphi_{Cys} = -90^{\circ}$ i $\psi_{Cys} = -60^{\circ}$ dla cysteiny, b) $\varphi_{His} = -60^{\circ}$ i $\psi_{His} = -85^{\circ}$ dla histydyny oraz $\varphi_{Cys} = \psi_{Cys} = -60^{\circ}$ dla cysteiny

In the model we get the following sequence of amino acids:

```
 1  ASN SER TYR PRO GLY CYS PRO SER SER TYR ASP GLY TYR CYS LEU
16  ASN GLY GLY VAL CYS MET HIS ILE GLU SER LEU ASP SER TYR THR
31  CYS ASN CYS VAL ILE GLY TYR SER GLY ASP ARG CYS GLN THR ARG
46  ASP LEU ARG TRP TRP GLU LEU ARG
```

Next, using standard force field parameters AMBER [CCBG95, Pond01, Atki98, Lide03] for protein synthesis, and generating amino acid chain without torsion we get the protein EFG in

PDB format (the EGF protein in PDB format is presented in Appendix IV). Fig. 4.10 shows the RasMol representation of straight protein EGF. In the case, when we assume the torsion angles φ and ψ in a peptide bond for glycine in all places where they are placed in the chain equal –45°, the spatial folded protein shape [ZnZu02b] gets the form presented in Fig. 4.11.

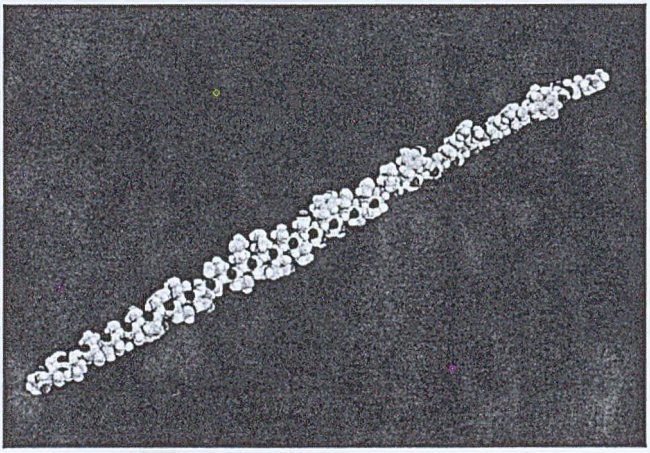


Fig. 4.10. The RasMol representation of straight protein EGF. Spacefill representation of molecule
Rys. 4.10. Rozciągnięta proteina EGF w reprezentacji programu RasMol. Reprezentacja kulowa molekuły

Fig. 4.11. The spatial shape of folded protein EGF
Rys. 4.11. Przestrzenny kształt proteiny EGF

4.2.2. Determining the Free Conformation by Dynamic Programming

Based on Fig. 4.7 we assume that the first amino-acid residue in the peptide chain has a number 0, the next is 1 and so forth. The Bellman's dynamic programming [Bell57, TaKu71]

we'll use to determine the torsion angles chain (4.1) in the polypeptide to be formed [ZnZu03, WeWZ03b].

Let us denote the potential energy function [LHSD95] of the 0^{th} amino-acid residue by E_0. We can to accept the assumption that the potential energy is a function of torsion angles φ_0 and ψ_0. The shape of the backbone of the polypeptide chain depends only on the pairs of the φ and ψ angles, because ω is usually equals 180° and χ is void.

As a consequence, the energy of the first residue of the peptide chain can be expressed as:

$$E_0 = E_0(\varphi_0, \psi_0). \tag{4.2}$$

We will quantize the E_0 for $\varphi_0 = \{\varphi_0^0, \varphi_0^1, \ldots \varphi_0^K\}$ and $\psi_0 = \{\psi_0^0, \psi_0^1, \ldots \psi_0^L\}$. Therefore we have:

$$E_0^{k,l} = E_0^{k,l}\left(\varphi_0^k, \psi_0^l\right).$$

The grid is not fully filled because of the Ramachandran restrictions.

When the residue of next (i.e. 1^{st}) amino acid appears, the minimal energy of the bonded residues of amino acids 0 and 1 has the form:

$$E_1^{k,l}\left(\varphi_1^k, \psi_1^l\right) := \min_{k,l}\left(E_0^{k,l} \Rightarrow E_1^{k,l}\right). \tag{4.3}$$

where symbol $\Rightarrow$ denotes the computation of the total energy in the point $E_1^{k,l}$ reached from points $E_0^{k,l}$ $(k = 1,2,\ldots K, l = 1,2,\ldots L)$, and symbol := denotes computation of the right-hand side expression (4.3) and assigning the result to the left-hand side.

When the residue indexed as the 2^{nd} appears, the minimal energy for the three bonded residues of amino acids (in all accessible points on a grid) has the form:

$$E_2^{k,l}\left(\varphi_2^k, \psi_2^l\right) := \min_{k,l}\left[\min_{k,l}\left(E_0^{k,l} \Rightarrow E_1^{k,l}\right) \Rightarrow E_2^{k,l}\left(\varphi_2^k, \psi_2^l\right)\right]. \tag{4.4}$$

When we reach the last n^{th} residue, we have:

$$E_n^{k,l}\left(\varphi_n^k, \psi_n^l\right) := \min_{k,l}\left[\min_{k,l}\left(E_{n-2}^{k,l} \Rightarrow E_{n-1}^{k,l}\right) \Rightarrow E_n^{k,l}\left(\varphi_n^k, \psi_n^l\right)\right]. \tag{4.5}$$

This is the key point of the procedure, for $\min_{k,l} E_n^{k,l}\left(\varphi_n^k, \psi_n^l\right)$ in (4.5), when we get back to the E_0, we can find the optimal "trajectory" (minimal energy) for the set of pairs (φ_i, ψ_i) in the form:

$$(\varphi_n, \psi_n)_{opt} \rightarrow (\varphi_{n-1}, \psi_{n-1})_{opt} \rightarrow \quad \ldots\ldots \quad \rightarrow (\varphi_0, \psi_0)_{opt}, \tag{4.6}$$

and the conformation (4.1) of the backbone of the peptide chain is determined.

The procedure is illustrated in Fig. 4.12.

In the course of the procedure of determining of the trajectory (4.6), the condition of existing hydrogen or disulfide bond has to be checked. When the condition is fulfilled, the sub-backbone is fixed, and the minimization is continuing, but the optimal part of the sub-backbone stays unchanged.

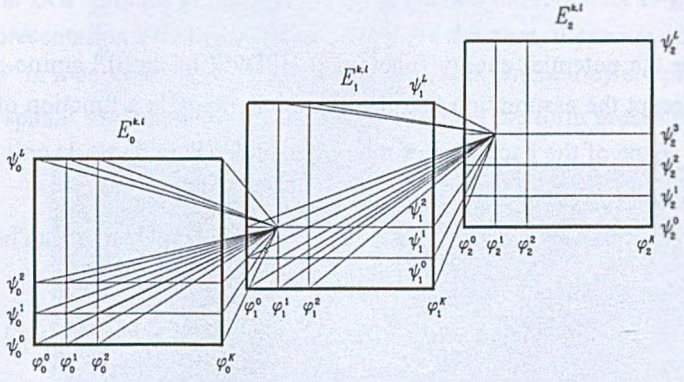


Fig. 4.12. Conformation determined by dynamic programming (steps 0 to 2)
Rys. 4.12. Wyznaczanie konformacji metodą programowania dynamicznego (kroki 0 do 2)

An illustration of presented algorithm is a computation of the free conformation of the polypeptide (named A) containing seven amino acids in a sequence [HeZZ03a]:

Methionine – Alanine – Glycine – Histidine – Glycine – Alanine – Histidine

By assuming that atoms behave as hard spheres, allowed ranges of torsion angles can be predicted and visualized in contour diagrams of Ramachandran plots (Fig. 4.13). Today, more than 30 years after the introduction of the Ramachandran plot, the quality of protein structures determined by X-ray crystallography is such that it is possible to verify and slightly modify the exact shapes of the allowed regions in classic plot. It has practical aspect in the prediction of the protein conformations (Fig. 4.14).

The determined set of pairs (4.6) for the polypeptide A with Ramachandran's restrictions from Fig. 4.14, is presented in Fig. 4.15a, yet the spatial shape of the folded polypeptide A in Fig. 4.15b. The structure of this polypeptide in PDB format is presented in Appendix IV.

4.2.3. Conformation Switching

When the translation process reaches the last, termination stage, the chain of amino-acid residues forming the polypeptide is inserted into an environment.

The polypeptide forms a chain of the molecules of residues connected together through the rotational bond realized by peptide bonds. A tendency of the chain of polypeptide to get minimal conformational energy [LHSD95, GuWu01], is a reason of forcing the changes. This can be called free conformation of the polypeptide chain.

In the case when an external force influences on the polypeptide chain (e.g. chaperons or enzymes) that extended system also tends to reach minimal internal energy. This can be called a forced conformation. In this case (Fig. 4.16) possible conformation depends on mutual interaction between residues of amino acids and molecules and parameters of the environment

e.g. pH, chemical cutting or chaperones' affecting. It is important that the internal bonds e.g. disufide bonds or hydrogen bonds can interrupt the conformation transient state.

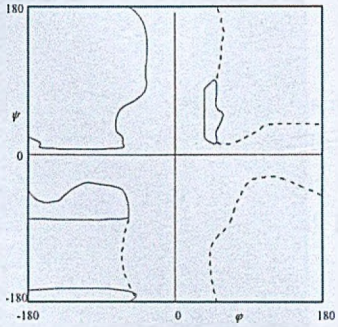


Fig.4.13. The classical version of the Ramachadran plot [Rama68, Stry94] for L-alanine residues (or any amino acid except glycine and proline) – solid line. Additional conformations are accessible to glycine (dashed line). A proline residue has a markedly restricted range because of its special shape

Rys.4.13. Klasyczny wykres Ramachandrana [Rama68, Stry94] dla reszt L-alaniny (lub każdego innego aminokwasu z wyjątkiem glicyny i proliny) – linia ciągła. Dodatkowe obszary możliwych konformacji dla glicyny oznaczono linią przerywaną. Obszar dopuszczalny dla proliny jest znacznie ograniczony ze względu na specyficzny kształt boczny jej reszty

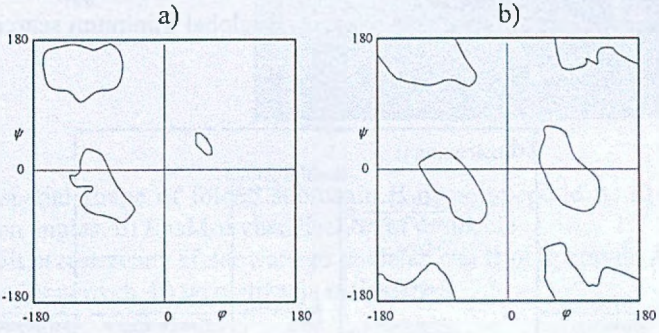


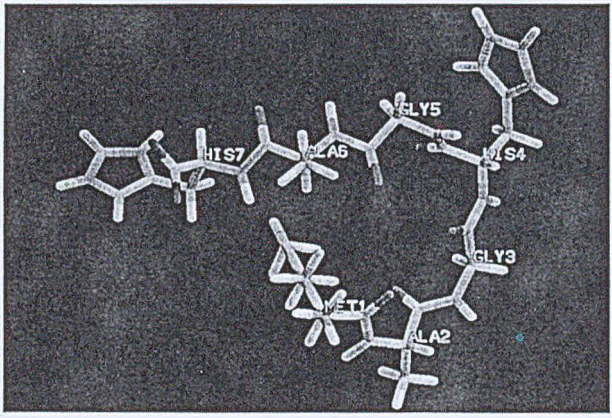
Fig. 4.14. Experimentally observed Ramachandran plots for alanine and all 19 non-glycines (a) and glycine (b). Experimental plots were made for 237 384 amino acids in 1042 protein from the PDB database [HoZO02]

Rys. 4.14. Obszary Ramachandrana dla alaniny i łącznie 19 aminokwasów z wyjątkiem glicyny (a) oraz glicyny (b). Wykresy eksperymentalne znaleziono po zbadaniu 237 384 aminokwasów w 1042 białkach z bazy danych PDB [HoZO02]

In Fig. 4.16 the two main groups of post-translational modifications are presented: firstly the chemical modifications based on exchange of side-chains in a polypeptide chain and cutting of the selected amino acids, and secondly, conformation modifications caused by e.g. pH,

chaperones leading to determining the set of protein torsion angles in the amino-acid sequence.

Chain of amino acids	Torsion angles φ_i	ψ_i
Met	-67°	135°
Ala	-65°	136°
Gly	91°	-180°
His	-68°	135°
Gly	88°	-180°
Ala	-151°	145°
His	-102°	131°



a) b)

Fig. 4.15. The spatial shape of folded polypeptide A: a) the chain of torsion angles, b) RasMol visualization of a molecule

Rys. 4.15. Przestrzenny kształt polipeptydu A: a) łańcuch kątów torsyjnych, b) wizualizacja

A major disadvantage of dynamic programming in determination of a polypeptide conformations in case of high accuracy of computations is the excessive computer-memory requirement, however this approach can be used in global minimum searching for conformational energy of polypeptide.

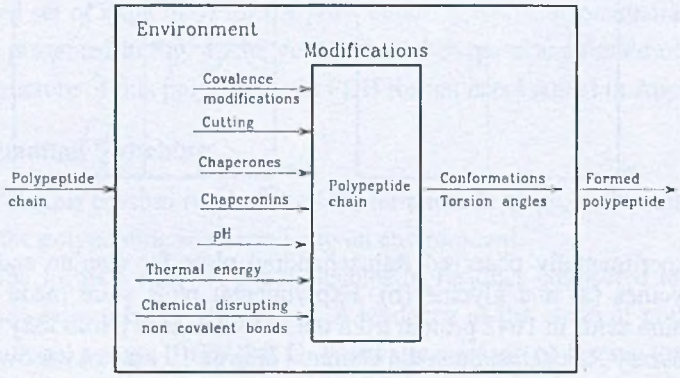


Fig. 4.16. Determination of the torsion angles as a result of the interaction of a polypeptide chain and the environment

Rys. 4.16. Wyznaczanie kątów torsyjnych ustalanych w wyniku interakcji łańcucha polipeptydu i środowiska

The alternative approach based on modified Monte Carlo method [MeUl49] (in this case, the computations are highly time-consuming) in the energy-based conformation determining of polypeptide chains is presented in [WaZn04a, WaZn04b].

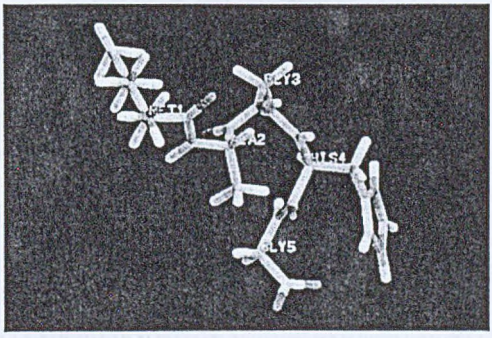
4.2.4. Cleavage of Chain

The cleavage mechanism also called cutting (Fig. 4.16) is an irreversible process of cutting of the long nanostructures (like a peptide sequences) into sub-chains with the basically different properties than the sub-chains inside the origin. The reason is the switching of its conformations to the new shapes. An illustration of cleavage process is determining of the sub-chain B conformation as a part of the polypeptide A (Fig. 4.15). The sub-chain B contains five amino acids in the sequence:

Methionine – Alanine – Glycine – Histidine – Glycine

The determined set of pairs (4.6) for sub-chain B is presented in Fig. 4.17a, yet the spatial shape of the folded, B sub-chain of polypeptide A in Fig.4.17b.

Chain of amino acids	Torsion angles φ_i	ψ_i
Met	-66°	134°
Ala	-104°	130°
Gly	-67°	-47°
His	-102°	131°
Gly	65°	-48°



a) b)

Fig. 4.17. The spatial shape of folded sub-chain B of polypeptide A: a) the chain of torsion angles, b) RasMol visualization of molecule

Rys. 4.17. Kształt przestrzenny sfałdowanego podłańcucha B polipeptydu A: a) łańcuch kątów torsyjnych, b) wizualizacja molekuły

The PDB files describing of polypeptide A and sub-chain B are presented in Appendix IV.

For exploration of polypeptide folding in the nascent polypeptide chain (in elongation phase) and investigation of the conformation switching of polypeptide in the cleavage of chain process performed in the nascent protein chain (Fig. 4.2), the new two-phase NPF (Nascent Protein Folding) Simulation Algorithm was developed [ZnZn04, Znam04]. In NPF algorithm, the simulation process retains the same sequence of events as a real process of nascent protein elongation. The algorithm description is presented in Appendix IV. An illustration of this algorithm are the simulation results of elongation process and configuration

changes caused by cleavage of the chain of eight amino acids from the origin of the nascent, twelve amino acids chain:

```
asn-ser-tyr-pro-gly-cys-pro-ser-ser-tyr-asp-gly
```

The whole, twelve amino acids chain folded in the nascent phase is presented in Fig. 4.18.

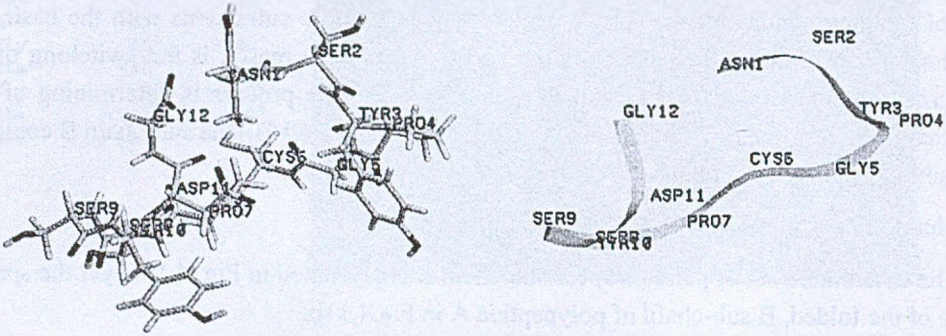


Fig. 4.18. Conformation of the twelve amino acids polypeptide: a) sticks representation of the structure, b) ribbons representation

Rys. 4.18. Konformacja łańcucha dwunastu aminokwasów polipeptydu: a) reprezentacja belkowa, b) reprezentacja wstęgowa

The switched conformation of the eight amino acids sequence:

```
asn-ser-tyr-pro-gly-cys-pro-ser
```

as a part of the nascent protein caused by the cleavage of the origin chain is presented in Fig. 4.19.

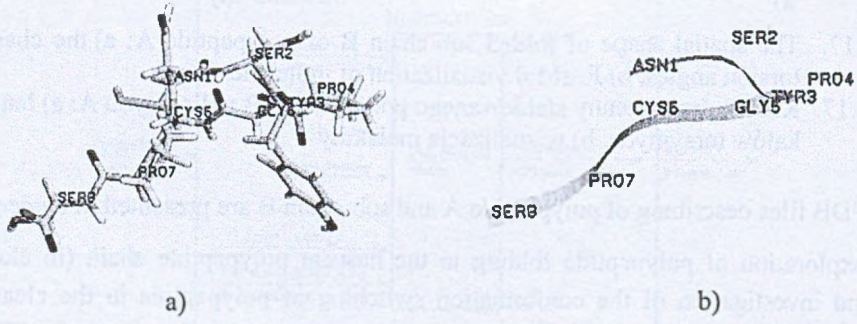


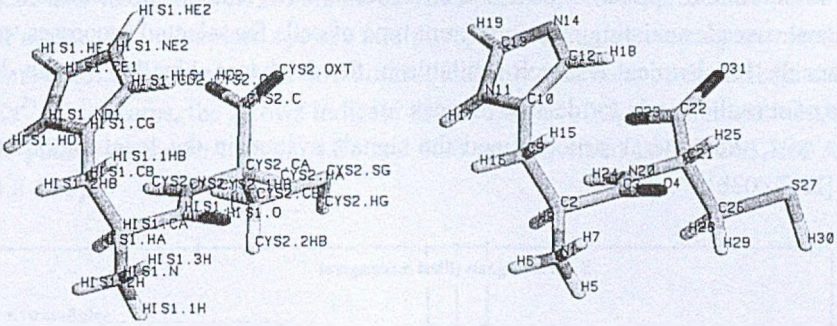
Fig. 4.19. Conformation of the eight amino acids polypeptide after cleavage: a) sticks representation of the structure, b) ribbons representation (compare with Fig. 4.18b)

Rys. 4.19. Konformacja odciętego łańcucha ośmiu aminokwasów polipeptydu: a) reprezentacja belkowa, b) reprezentacja wstęgowa (por. rys. 4.18b)

4.2.5. pH Changes

The interaction of environment parameters with a nanostructure leads to the conformation switching. In case of bio-nanostructures like polypeptides, the activities of many proteins are modulated by pH through protonation of amino acid of histidine side chain. In result of protonation, the distribution of charge in molecule is changed and this leads to the conformation switching.

The resultant conformation can be computed through modification of molecule model covered in its PDB [BWFG00, Nucl01a, Klot01] file. The computation can be performed similarly to the previous description. In Fig. 4.20, the structural change of the dipeptide histidine-cysteine molecule is presented by RasMol program, in the dependency on the pH of molecule environment.



a) b)

Fig. 4.20. Change of the charge of histidine side chain in the his-cys dipeptide: a) pH 5.8, b) pH 7.8

Rys. 4.20. Zmiana ładunku łańcucha bocznego histydyny w dipeptydzie his-cys: a) dla pH wynoszącego 5.8, b) dla pH wynoszącego 7.8

The conformations presented in Fig. 4.20 are optimized in energetic sense, and the torsion angles sequences determining the switched, spatial shape of molecules are respectively:

$$\left(-63.0°,154.0°\right)_{his} \rightarrow \text{PB} \rightarrow \left(-115.0°,112.0°\right)_{cys},$$

and

$$\left(-61.0°,143.0°\right)_{his} \rightarrow \text{PB} \rightarrow \left(-145.0°,145.0°\right)_{cys}.$$

Symbol PB denotes the peptide bond.

4.3. Signaling Switching

Appeal to biocompatible nanoprocesses it deems that the detecting and moving of stimuli information are processed by signal transduction cascades. Those molecular circuits mediate, store, amplify, transfer and process diverse internal and external signals.

This section discusses the properties of signaling switching in the signal transduction cascades observed in the nanonetworks based on selected biological examples [Berr85, BioC03, LBZM01, Stry94].

4.3.1. Nanonetworks

Generally, we can talk about wide area and local nanonetworks. In living organisms, an electro-chemical net (e.g. nervous system) and extracellular communication net (e.g. immune and hormone systems), represent wide area nanonetworks [Tone85, Snyd85].

A cell represents a local area nanonetwork. One of the most natural (but not simple) approach to build the local nanonetwork performing a desired production process, which can be modified through the external control, is exploitation of a living cell. The fundamental condition, which have to be fulfilled for the cell, is an assurance of survival requirements. The control needs stimulation of inputs of the signal cascades in a cell from its environment.

The signal cascades existing in the different type of cells for selected processes, can be retrieved from the biochemical research available in the databases. Finally, we can determine a sequence of stimuli signals for desired process.

In Fig. 4.21, the general structure and the signals system in the local nanonetwork are presented [HeZZ03b].

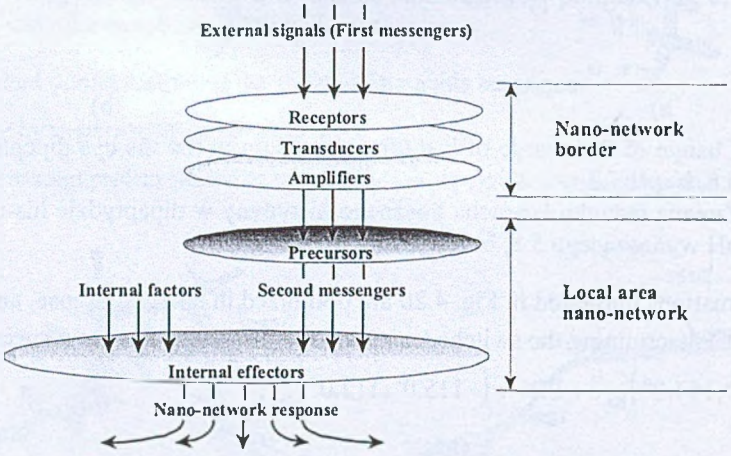


Fig. 4.21. Signals system level in a local nanonetwork
Rys. 4.21. Poziom sygnałów systemu w lokalnej nanosieci

4.3.2. Hierarchical Description of Nanonetworks

The signal cascades in nanonetworks are usually demonstrated for selected processes, which can be easily and precisely described during the biochemical analysis. However, in realty, we have to consider interdependent, multi-process systems. In this case, a use of hier-

archy can be helpful. A level of hierarchy describes the phenomena taking place in the process with a different rank of particularity. Namely, we can talk about a signals system level, a signal cascade pathways level, a graph network level and a quantitative level.

Signals System Level

In Fig. 4.21 the *signals system level* for the local nanonetwork is presented. First messengers are the external signal molecules arriving at receptor molecules on the border of a nanonetwork (e.g. plasma membrane of the cell). Second messengers are signal molecules in the interior of the local nanonetwork (e.g. in the cell, these are: cyclic adenosine monophosphate – cAMP, diaglycerol – DAG or inositol triphosphate – IP_3).

Signal Cascades Pathways Level

Figs. 4.22 and 4.23, illustrate the *signal cascade pathways level*, presented for two fundamental cell's cascades; adenylate cyclase and phosphoinositide converting extracellular signals into intracellular ones, which in turn control multiple functions of the cell (kinases A, C, and ions Ca^{2+}). In figures, the arrows indicate the directions of signals transduction. The signal cascade pathways shown in Figs. 4.22 and 4.23 are described in [BioC03, see Appendix IV – p. 6.4.8 also].

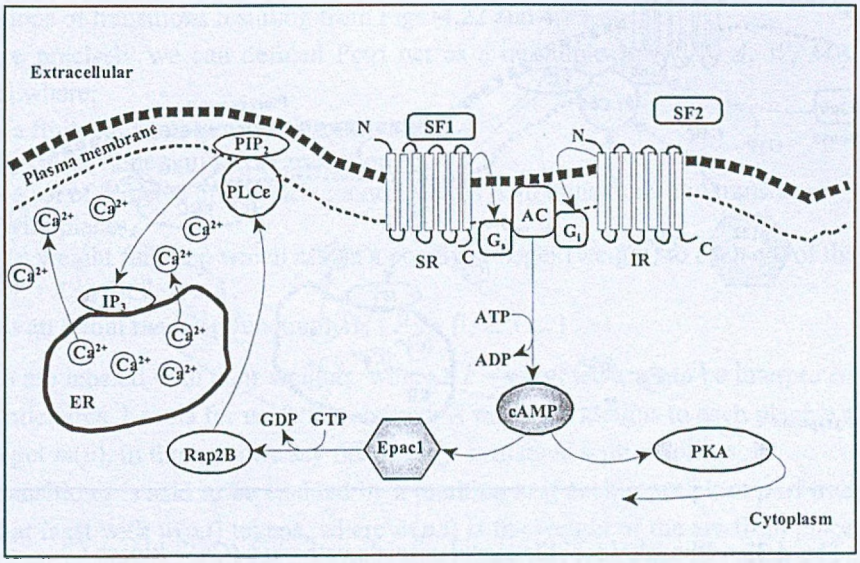


Fig. 4.22. Adenylate cyclase signal cascade pathways (Ca^{2+}, kinase A)
Rys. 4.22. Ścieżki kaskady sygnałowej cyklazy adenylanowej (Ca^{2+}, kinaza A)

Symbols in Fig. 4.22, denote the following compounds:
SF1 – stimulatory factor (stimulatory messenger molecule),

SR – receptor for stimulatory messenger (cell-surface receptor),
SF2 – inhibitory factor (stimulatory messenger molecule),
IR – receptor for stimulatory messenger,
G_s – stimulatory G protein complex,
G_i – inhibitory G protein complex,
AC – adenylyl cyclase (adenylate cyclase),
ATP – adenosine triphosphate,
ADP – adenosine diphosphate,
cAMP – cyclic AMP (adenosine monophosphate),
PKA – kinase A,
Epac1 – activating protein,
GTP – guanosine triphosphate,
GDP – guanosine diphosphate,
Rap2B – member of RAS protein family, small GTP-binding protein, which leads to PLCε activation,
PLCε – phosphoinositide-specific phospholipase C PLCε (enzyme which catalyses the hydrolysis of membrane phospholipids and produces a second messenger inositol triphosphate (IP_3)),

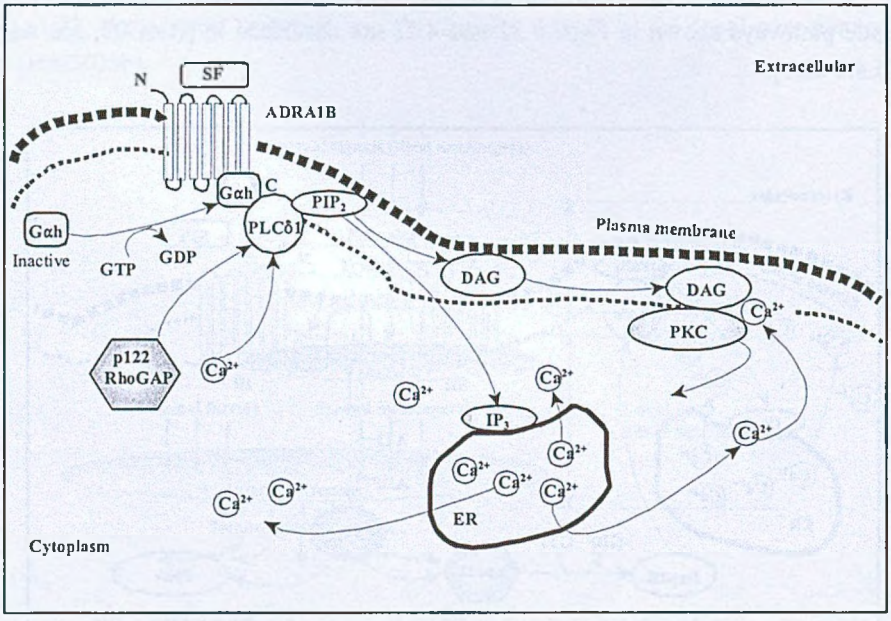


Fig. 4.23. Phosphoinosidite signal cascade pathways (Ca^{2+}, kinase C)
Rys. 4.23. Ścieżki kaskady sygnałowej fosfoinozytolu (Ca^{2+}, kinaza C)

PIP_2 – phosphatidylinositol biphosphate,
IP_3 – inositol triphosphate,
Ca^{2+} – calcium ions,
ER – endoplasmic reticulum.

Symbols in Fig. 4.23, denote the following compounds:

SF – stimulatory factor (stimulatory messenger molecule),
ADRA1B – cell-surface receptor,
Gαh – GTP-binding protein acticated by GTP, known as transglutaminase,
GTP – guanosine triphosphate,
GDP – guanosine diphosphate,
p122RhoGAP – activating protein,
PLCδ1 – phospholipase C (PLC) δ1 (enzyme which produces two second messengers, diacylglycerol (DAG) and inositol triphosphate (IP_3)),
PIP_2 – phosphatidylinositol biphosphate, the membrane lipid hydrolyzed by phospholipase PLCδ1,
DAG – diacylglycerol,
IP_3 – inositol triphosphate,
Ca^{2+} – calcium ions,
PKC – kinase C,
ER – endoplasmic reticulum.

Graph Network Level

The signal cascades from Figs. 4.22 and 4.23 are fused in Fig 4.24, representing the *graph network level*, in a form of extended Petri net [Mura89]. Places are expressed by circles, transitions by bars, inhibitor arcs have small circles instead of arrows, the initial marking is represented by dots inside circles, and the firing rate and choice functions are given as additional descriptions of transitions resulting from Figs. 4.22 and 4.23.

More precisely we can defined Petri net as a quintuple $N=(P, T, A, W, M_0)$ [Mura89, Zube85] where:

P is a finite, nonempty set of places,
T is a finite, nonempty set of transitions,
A is a set of directed arcs which connect places with transitions and transitions with places,
W is a weight function which assign a positive integer (weight) to each arc of the set, $W : A \rightarrow \{1, 2, 3, \ldots\}$,
M_0 is an initial marking function, $M_0 : P \rightarrow \{1, 2, 3, \ldots\}$.

Arcs are labeled with their weights, where a k – weighted arc can be interpreted as the set of k parallel arcs. Labels for unity are omitted. A marking, assigns to each place p a nonnegative integer $m(p)$, in this case we say that place p is marked with m tokens.

A transition t is said to be enabled by a marking m if each input place p of transition t, is marked at least with $w(p,t)$ tokens, where $w(p,t)$ is the weight of the arc from place p to transition t, i.e. $m(p) \geq w(p,t)$. Every transition enabled by a marking m can fire. When an enabled transition t fires, tokens are removed from t's input places in numbers corresponding to the weights of input arcs, and similarly, the weights of t's output arcs determine the numbers of token added to output places.

An inhibitor arc connects a place to a transition and is shown by a line terminated with a small circle at the transition. The inhibitor arc disables the transition when the input place has

a token and enables transition (for this input) when input place has no token. No tokens are moved through an inhibitor arc when the transition fires.

The symbols in Fig. 4.24 and symbols from Figs. 4.22 and 4.23 are related by:

places:

p_1 – SR, p_2 – IR, p_3 – ATP, p_4 – GTP, p_5 – PIP_2,
p_6 – ADRA1B, p_7 – p122RhoGAP, p_8 – G_s,

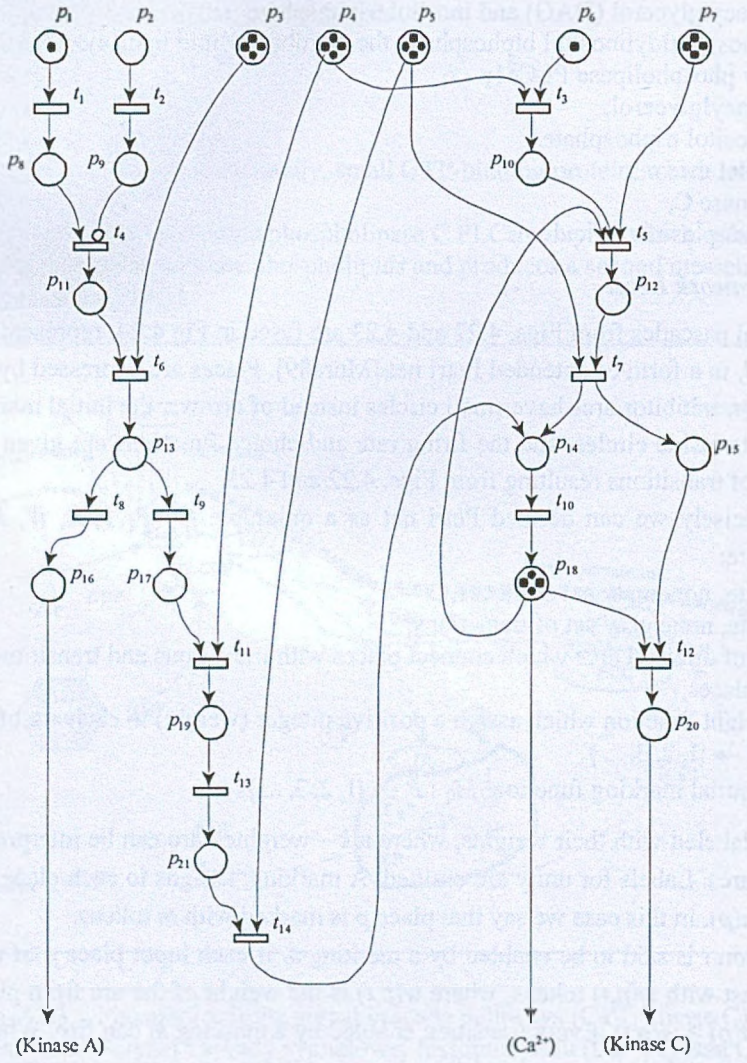


Fig. 4.24. Signal cascades of adenylate cyclase and phosphoinositide in a fused form of a Petri net

Rys. 4.24. Fuzja kaskad cyklazy adenylanowej i fosfoinozytolowej w postaci sieci Petri

p_9 – G_i, p_{10} – Gαh, p_{11} – AC, p_{12} – PLCδ1, p_{13} – cAMP,
p_{14} – IP_3, p_{15} – DAG, p_{16} – PKA, p_{17} – PIP_2, p_{18} – Ca^{2+},
p_{19} – Rap28, p_{20} – PKC, p_{21} – PLCε.

external input signals:
SR, IR, ADRA1B

signals, that could be stimulated from the other signal cascades:
ATP, GTP, PIP_2, p122RhoGAP

nanonetwork response:
Kinase A, Kinase C, Ca^{2+}.

When the fused net is very complex, its feature can be explored by the theory of Petri nets or analyzed by a computer program. In the signal cascades analysis, the liveness of a net is critical, because the dead branches or deadlock can degrade the functionality of the considered signal cascades [Mura89, Zube85].

The selected cases of a lack of liveness of a Petri net are illustrated in Fig. 4.25a and 4.25b.

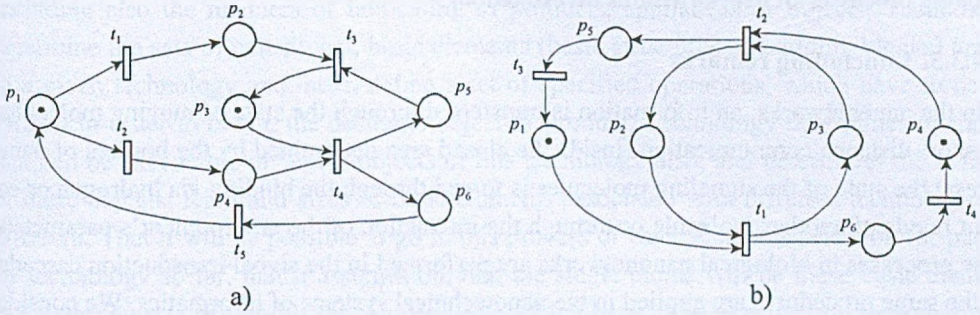


Fig. 4.25. Liveness of a Petri net: a) a dead branch (if t_1 fires first), b) deadlock
Rys. 4.25. Osiągalność w sieci Petri, a) martwa gałąź (gdy tranzycja t_1 zajdzie wcześniej niż tranzycja t_2), b) blokada

Quantitative Level

The kinetics of reactions is presented at the *quantitative level*. In this case, the models like of Michaelis-Menten's one can be used for description of some enzymatic reactions. The composite reactions are investigated through a computer simulation (e.g. GEPASI 3 program [Mend99], if it is applicable for a discussed signal cascade).

At the quantitative level, for the purpose of a fundamental steady-state analysis, four formulas are used to express the chemical composition of chemical compounds: empirical, molecular, structural and conformational. *Empirical formula* determines the types of atoms present and the ratio of atoms - but not the actual numbers of atoms present in the molecule. The *molecular formula* shows the exact numbers and types of elements in the molecule. Therefore,

the molecular formula provides us with more information than the empirical one does. However, molecular formulas do not tell us how atoms are joined together in the molecule. In order to understand the interdependent arrangement of atoms in a molecule, we must employ a *structural formula*. The structural formula shows the exact types and numbers of atoms appearing in the molecule and also how the atoms are chemically bound to one another.

The most adequate for computer processing is the fourth, *conformational formula*, as expressed in different file format descriptions (see p. 4.1.1) as PDB (Protein Data Bank) [Nucl01a], mmCIF (macromolecular Crystallographic Information File) [Nucl01b], NCBI-Entrez-rotein (sequence database) [NCBI03], NCBI-Entrez-Nucleotide (sequence database [GenBank]) [BBLO99], and others. In case of mmCIF, information about the molecule is very detailed and describes not only a chemical structure in a broad sense (e.g. internal geometry, average values for the bonds, angles and torsions in the structure, polarizability and hydrophobicity), but also contains the adequate information about the macromolecular crystallographic examination together with its results.

The hierarchical description of the nanonetworks signal transduction with the conformational formula applied in this chapter seems to be the most effective description for the switching processes of nanostructures investigations.

4.3.3. Concluding remarks

In the nanonetworks, an information is transferred through the state of moving molecules. In a short-distance communication (inside the closed area determined by the borders of nanoprocess) the state of the signaling molecules is forced through the binding via hydrogen or covalent bonds of another molecule or through the interaction of the environment's parameters. These processes in biological nanonetworks are performed in the signal transduction cascades and the same procedures are applied in the nanotechnical systems of informatics. We considered these processes with emphasis on the fusion of cascades.

In general, these interactions lead to the switching of conformations of the molecule. In this chapter, we focused on biocompatible nanostructures introducing the standard, formal description of molecular structures, methodology of modeling and simulation of the conformational changes, and hierarchical description of nanonetworks useful in the switching conformation studies. The simulation methodologies based on the dynamic programming, Monte Carlo and Nascent Protein Folding algorithms are investigated. Moreover, nanotechnological, two-stage production processes based on the "gluey matrix" concept are discussed.

5. CONCLUSIONS

Informatics is a discipline of science exploring the laws of processes of coding, processing, storing and transferring information or data. In the physical implementation of these phenomena we have to consider the type of technology used to build the elements and objects representing a working system.

Generally, a technology determines the manners of solving of classes of the definite tasks including also the manners of fabricating of products, appliances or objects. Technologies determine the sets of constituent, basic elements (basic structures or building blocks) applied in a given technology and, next, define a set of specified operations, which have to be performed in order to obtain the desirable object or product. Technology determines operations that can be executable on active objects of this technology also, and determines the behavior of these objects. Kind and sizes of basic elements associated with different technologies are different. That it will be possible to go in this process of basic elements selection for particular technology so far, that it assumes on, that the single atoms will be these basic elements. But then, the size of the full set of operations, which have to be executed on these basic elements in order to receive the final object with desirable features, it will be excessive. In summary, and it is possible to say without care about precision, that dimensions of basic elements accepted in given technology are inversely proportional to the number of operations, which are necessary to execute on them in order to receive the desirable object. So, the choice is basic case and elaboration of such basic elements, which have decreased the number of necessary operations to execute considerably, in order to receive the required final result. Then, it is possible to say about switching between these elements accepted as basic elements, in order to structures have built about the desirable properties including also the dynamic changes of those properties. It is possible to describe the process of fabricating of these structures on the regulation of smallest elements connections, but there is not enough effective, better when the basic elements are extended more and the processes of switching determine them functions.

This is a general principle it looks to be, which meaning may be shown in case of various tasks, appliances or products, which have to be performed. The works pay attention on it concerning the information processing, that it is a good practice to record the processed informa-

tion in such a partial sets, which will allow on the interesting results effectively received. There will be the vectors in case of mathematical tasks, registers with multiconductor transmission lines in case of digital techniques, structure configurations in the reprogrammable electronic circuits, and conformations of molecule chains in nanostructures, but the operations are executed on these partial sets. In technical implementation, these operations come down for switching of basic elements and require a precise grasping and analysis of critical features of these processes.

Switching is exhibited in different technologies by different basic elements. The idea of this work has resulted from there, that dealing in turn with so different cases as VLSI structures, FPAA structures and nanostructures, it is possible to notice, that the common feature takes a stand in solving the tasks related with them, rely on choice of certain basic elements critical for structure behavior as e.g. MTL, configurations of FPAA substructures or whole FPAA systems, molecule conformations, and it is operated on them but on the basic elements not ultra small analyzing the internal switching processes.

The movement and processing of information is indissolubly connected with the switching of states of structures carrying the data. In general, the changes of structure state can be forced through the changes of carried data parameters with unchanged structure configuration, through the switching of structure configuration or switching of the structure conformation.

In the work, the selected, basic problems of switching in digital VLSI technology, reprogrammable analog arrays FPAA technology, and nanotechnology have been discussed. Basing on the experimental and simulation results obtained, the practical conclusions can be used in analysis and design of a switching structures with CAD/CAE tools.

Switching in the Interconnections of Monolithic VLSI Structures. The quality measure of the designed VLSI structures, for most integrated circuits is a speed at which they perform their operations. In practice, the problem of on-chip interconnects between multi-bit VLSI macrocells structures is complex, because the data between macrocells are sent in a form of multi-bit words forming interconnections like busses, or in other words the coupled, multiconductor transmission lines. The fundamental parameters for matrix description (or modeling, simulation and design) of MTL include the capacitance matrices. Precisely, these are the matrices-per-unit of length, the capacitance coefficient matrix called Maxwell matrix of MTL and the two-terminal capacitance matrix. If the two-terminal matrix is known, the Maxwell matrix used for MTL switching characteristics estimation, can be computed from the two-terminal matrix. In the work, two methods of determination of the Maxwell matrix from measurements are presented: passive, indirect measurements and measurements with active separation. The measurements were performed basing on design and fabricated test structures ST2 and AF4. Experiments and accuracy analysis indicates that the computations of Maxwell matrix from passive measurements is strongly corrupted by the measuring errors and error propagation. Using indirect measurements to finding Maxwell matrix elements requires ex-

tremely high accuracy, that is, accuracy of instrument and carefully constructed measurement station. The algorithm for improved measurements of the two-terminal matrix (per-unit-length) of MTL developed in the work applies the measuring technique based on active separation of the capacitance network implemented using a high quality unity-gain voltage amplifier. The active separation significantly increases the accuracy of determining the Maxwell matrix in comparison with the indirect method. The symmetry of transformations of the Maxwell matrix and the two-terminal capacitance matrix plays a crucial role in the minimization of errors. It is shown that using the described method the accuracy of determining Maxwell's matrix coefficients is the same as the measurement accuracy of the two-terminal capacitances.

Developed in the work CAD tools for scaling (in geometrical sense) of MTL for its energetical characterization and so called diagonal matching method can be used for proper design of MTL working with high-speed switching.

Finally, the model of the dielectric absorption built on the measurement data has been presented. In the simulation experiments for longer interconnections (for given technology), it can be observed strong influence of dielectric absorption for the microstrip lines on degradation of switching characteristics in a VLSI structures of small geometry.

Switching in the Reprogrammable FPAA Structures. There are two main weak points in fast switching of reconfigurable FPAA: firstly, the time of download of the configuration from supporting program or EEPROM memory together with the time of transients in a FPAA chip when the download is finished and the chip undertakes its function, and secondly, for recently accessible FPAAs, there is no possibility of switching its parameters values and a part of active structure on-the-fly (during FPAA operation).

In the work, the solution of a very fast switching of the part of working FPAA is presented. The solution is based on external control of one or few CAB in the working FPAA without the download process. The measurements indicate that the new technique of switching of the CAB cell's mode in the selected cells, dramatically improved the dynamics of switching in the reconfiguration process of the FPAA chip. In case of single controlled amplifier (Track/Compute integrator) the transient time of switching is approximately 3μs, in switching of the linear macro structure requires not more than 5μs, and for non-linear macros approximately 8μs conditions. In comparison with other methods of reconfiguration like the "hiding" of transients state in multi-chip FPAA system (we need approximately 600μs) or the FPAA downloading (from approximately 2s through serial communication port of PC computer for AN10E40 chip through 100ms for MPAA020 using EPROM accompanying the FPAA, while 30ms for AN10E40 using flash memory), the new technique speeds up over three order of magnitude the switching of configuration in FPAA chip.

The solution of the download time problem is based on parallelization of the FPAAs and "hiding" of the download time and the transient time after a download.

Finally, the applications of the modified, fast switched FPAAs systems for adaptive and predictive control with possible application in the microreactors control are discussed. Field Programmable Analog Arrays, coupled with microreactor technology promise to change the way plants are built, as well as the methods by which their processes are designed and controlled. Development of microreactors and micromixers is rapidly progressing due to factors such as elimination of scale-up procedures, higher precision of mixing and component contact surfaces, and minimization of processing hazards. The experiments were performed to optimize the reconfiguration process in applications of plant simulation in predictive control, and adaptive control. In case of plant simulation in predictive control, we validated the behavior of the two FPAAs and multiplexer system modeling the dynamic plant in the speeded up time scale. Experiments and validation of simulated plant were performed from *initial conditions* mode in first FPAA, *compute* mode in first FPAA (with parallely tracking by second FPAA) through start of downloading in first FPAA with parallel start to compute in second FPAA. The FPAA configurations consecutively downloaded, assure coping of the state vector in the plant model (which is changing with time). Non-critical transient state in *track* mode is better then 15μs. Transient state in switching the output signals in FPAA and multiplexer in not longer than 2μs. Imperfection of copying state variable reaches value approximately 1.5%. These imperfection can be easily improved by tuning the switches, multiplexer and control signal (start of download) operation. In case of FPAA system used in adaptive control the goal of measurements was calculation of the time of downloading of implemented reconfigurable controller with alternative transfer functions in AN10E40 chips and determination of the interval time "hiding" the dynamic imperfections during on-the-fly changes in the modes of FPAAs. The experiments showed that the transfer function can be changed approximately 30 times per second. The transient state after download process is not longer than 2ms for applied transfer functions realizing this adaptive controller.

Swiching in the Nanostructures. In the nanonetworks, an information is transferred through the state of moving molecules. In a short-distance communication (inside the closed area determined by the borders of nanoprocess) the state of the signaling molecules is forced through the binding via hydrogen or covalent bonds of another molecule or through the interaction of the environment's parameters. These processes in biological nanonetworks are performed in the signal transduction cascades and the same procedures are applied in the nanotechnical systems of informatics. We considered these processes with emphasis on the fusion of cascades.

In general, these interactions lead to the switching of conformations of the molecule. In the work, we focused on biocompatible nanostructures introducing the standard, formal description of molecular structures, methodology of modeling and simulation of the conformational changes, and hierarchical description of nanonetworks useful in the switching conformation studies. The simulation methodologies based on the dynamic programming, Monte

Carlo and Nascent Protein Folding algorithms are investigated. Moreover, nanotechnological, two-stage production processes based on the "gluey matrix" concept are discussed.

The hierarchical description of the nanonetworks signal transduction with the conformational formula and algorithms applied, seems to be the most effective description for the switching processes of nanostructures in the nanonetworks investigations.

Future works in range of technologies mentioned above will concern the process of synthesis understood as a choice of basic elements from a certain design space generally, and the proper switching operations those for the obtainment of the object or group of objects about required specificities including the switching operations caused by environmental stimuli.

6. APPENDICES

6.1. Appendix I – Test Structures ST2 and AF4

The test structures ST2 and AF4 were designed in Institute of Informatics at Silesian University of Technology (Gliwice) and fabricated at ITE (Institute of Electron Technology) in Warsaw, in a first round of ASIC/DI (Application Specific Integrated Circuits/Design and Implementation) Program [PiZn93, PiZn94], the Polish analog for MOSIS (MOS Implementation Service) in USA [MeCo80, NeMa83, Tomo88, Hein88], and EUROCHIP [Euro89, Euro91a-c] (EUROPRACTICE as a continuation [Euro95a-c, ESCI99]) in Europe.

The general goal of the Program i.e. to bridge a gap for students and research project prepared during the Lab course of ASIC/VLSI design at Universities and standard implementation at ITE as a Silicon Foundry was fulfilled. As a stimulated result of this action, was developing and mastering of the "interface" between designer and a Silicon Foundry. This interface is represented with a project transfer method, file transfer formats (CIF file for projects), design rules formalization and necessity to regulate the CAD tools for DRC, ERC, SPICE simulation models and HDL of projects description for ASIC/VLSI designers, assembled around ITE as a Silicon Foundry.

The test structures were designed [Znam93a, Znam93b] in a CIF format [MeCo80] basing on design rules, SPICE models of transistors and electrical data from ITE, as a standard cell's pattern was popular designer's library [NeMa83], and next, the projects were delivered by Internet to ITE. The DRC and final electric tests were performed in cooperation with ITE.

6.1.1. CIF Description of ST2 and AF4 Structures

The listing below, presents the CIF description of test structure ST2 containing coupled multiconductor transmission lines in metal layer, coupled interconnections in diffusion and polysicon layers and scaled (in dimensions) inverters structures. The ST2 structure is mounted in 28-pin CerDIP package. The CIF description of structure AF4 is reported in [L. Znamirowski, M. Skrzewski, T. Firlus, R. Pawłowski, J. Piasecki, S. Warecki: "CAD Systems for VLSI

Routing Design", Research Report BK-608/RAu2/93, Institute of Informatics, Silesian University of Technology, Gliwice 1993 (in Polish)]. AF4 contains logic circuits and long coupled multiconductor transmission lines. The AF4 die is mounted in 40-pin CerDIP package.

The layouts of ST2 and AF4 are presented in Figs. 2.19 and 2.16 respectively.

```
(ST2_StrukturaTes
towa2);

(PadIn4);
DS 205 125/1;
L ND;
B 4 192 14,116;
B 134 4 81,22;
B 16 26 22,185;
B 154 36 105,186;
B 8 16 150,28;
L NP;
B 150 4 93,178;
B 150 4 93,192;
B 8 8 22,204;
B 4 10 20,173;
B 4 16 20,200;
B 4 14 166,185;
L NC;
B 4 4 22,204;
B 8 4 36,200;
B 8 4 56,200;
B 8 4 76,200;
B 8 4 96,200;
B 8 4 116,200;
B 8 4 136,200;
B 4 8 150,30;
B 8 4 156,200;
B 8 4 176,200;
L NM;
B 200 16 100,8;
B 200 32 100,196;
B 108 108 100,106;
B 8 34 150,41;
L NG;
B 92 92 100,106;
DF;

(PadOut4);
DS 204 125/1;
L ND;
B 16 54 8,239;
B 200 56 100,28;
B 50 156 25,134;
B 20 8 22,262;
B 16 24 22,230;
B 12 8 24,276;
B 4 30 30,275;
B 24 4 42,232;
B 24 4 42,288;
B 100 56 100,184;
B 48 32 76,246;
B 32 14 68,283;
B 12 8 58,262;
B 12 10 72,225;
B 52 8 100,274;
B 48 32 124,246;
B 32 14 132,283;
B 12 10 128,225;
B 12 8 142,262;
B 24 4 158,288;
B 50 156 175,134;
B 16 8 164,234;
B 20 8 178,262;
B 4 30 170,275;
B 16 24 178,230;
B 12 8 176,276;
B 16 54 192,239;
L NI;
B 12 32 22,230;
B 12 16 22,262;
B 12 32 178,230;
B 12 16 178,262;
L NP;
B 180 4 100,20;
B 34 4 27,202;
B 4 184 12,112;
B 8 6 22,271;
B 4 56 22,242;
B 132 4 88,254;
B 148 4 100,36;
B 38 4 45,190;
B 4 156 28,114;
B 12 8 38,224;
B 4 18 42,217;
B 4 12 42,206;
B 106 4 101,238;
B 52 4 74,282;
B 12 8 58,224;
B 4 18 62,217;
B 4 24 62,200;
B 4 10 100,285;
B 42 4 133,282;
B 12 8 142,224;
B 4 18 138,217;
B 38 4 155,190;
B 4 24 138,200;
B 28 4 164,246;
B 4 28 152,268;
B 4 8 152,242;
B 12 8 162,224;
B 4 18 158,217;
B 34 4 173,202;
B 4 12 158,206;
B 4 156 172,114;
B 8 6 178,271;
B 4 56 178,242;
B 4 184 188,112;
L NC;
B 4 8 4,164;
B 4 8 4,130;
B 4 8 4,80;
B 4 8 4,32;
B 8 4 10,8;
B 4 8 20,56;
B 4 8 20,106;
B 4 8 20,156;
B 4 8 22,274;
B 8 4 30,8;
B 8 4 38,224;
B 8 4 50,28;
B 8 4 50,8;
B 8 4 58,262;
B 8 4 58,224;
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B 8 4 72,224;
B 8 4 76,208;
B 8 4 76,200;
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B 8 4 80,274;
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B 8 4 92,208;
B 8 4 92,200;
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B 8 4 100,274;
B 8 4 100,28;
B 8 4 108,208;
B 8 4 108,200;
B 8 4 110,8;
B 8 4 120,246;
B 8 4 120,274;
B 8 4 124,208;
B 8 4 124,200;
B 8 4 128,224;
B 8 4 130,8;
B 8 4 142,262;
B 8 4 142,224;
B 8 4 150,28;
B 8 4 150,8;
B 8 4 162,224;
B 8 4 162,234;
B 8 4 170,8;
B 4 8 178,274;
B 4 8 180,56;
B 4 8 180,106;
B 4 8 180,156;
B 8 4 190,8;
B 4 8 196,32;
B 4 8 196,80;
B 4 8 196,130;
B 4 8 196,164;
L NM;
B 8 154 4,93;
B 200 16 100,8;
B 200 32 100,196;
B 8 12 20,56;
B 8 12 20,106;
B 8 12 20,156;
B 8 12 22,274;
B 26 8 33,156;
B 26 8 33,106;
B 26 8 33,56;
B 12 8 38,224;
B 28 8 50,262;
B 8 40 40,240;
B 12 8 50,28;
B 8 22 50,41;
B 108 108 100,106;
B 26 8 65,224;
B 52 8 100,246;
B 52 8 100,274;
B 16 68 100,242;
B 12 8 100,28;
B 8 22 100,41;
B 26 8 135,224;
B 28 8 150,262;
B 12 8 150,28;
B 8 22 150,41;
B 26 8 167,56;
B 26 8 167,106;
B 26 8 167,156;
B 12 18 162,229;
B 8 30 160,245;
B 8 12 178,274;
B 8 12 180,56;
B 8 12 180,106;
B 8 12 180,156;
B 8 154 196,93;
L NG;
B 92 92 100,106;
DF;

(PadBlank);
DS 202 125/1;
L NM;
B 200 16 100,8;
B 200 32 100,196;
B 108 108 100,106;
L NG;
B 92 92 100,106;
DF;

(PadVdd);
DS 207 125/1;
L NM;
B 16 200 8,100;
B 40 108 32,100;
B 108 108 106,100;
B 36 16 34,54;
B 36 16 34,146;
L NG;
B 92 92 106 100;
DF;

(PadGnd);
DS 206 125/1;
L NM;
B 200 16 100,8;
B 200 32 100,196;
B 164 40 100,176;
B 16 36 54,178;
B 108 108 100,106;
B 16 36 146,178;
L NG;
B 92 92 100,106;
DF;

(PadClock);
DS 209 125/1;
L ND;
B 16 80 8,192;
B 8 8 30,224;
B 26 4 43,214;
B 16 22 38,299;
B 4 10 32,219;
B 8 8 42,282;
B 8 6 42,287;
B 4 20 44,270;
B 14 4 51,262;
B 8 8 48,240;
B 136 4 114,22;
B 8 12 50,30;
```

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B 14 4 57,238;
B 8 12 56,322;
B 4 34 54,305;
B 18 32 63,200;
B 4 30 58,277;
B 20 4 68,262;
B 8 12 66,304;
B 4 24 64,250;
B 32 16 80,208;
B 14 4 71,238;
B 12 32 74,308;
B 8 8 78,340;
B 8 8 80,264;
B 8 8 80,238;
B 4 8 80,332;
B 4 10 80,323;
B 18 8 89,320;
B 8 4 84,262;
B 4 36 82,222;
B 20 16 92,192;
B 12 16 92,256;
B 8 12 100,322;
B 8 114 100,253;
B 38 16 117,204;
B 18 8 111,320;
B 12 16 108,256;
B 8 4 116,262;
B 8 8 120,264;
B 8 8 120,238;
B 4 36 118,222;
B 8 8 122,354;
B 4 22 120,339;
B 4 10 120,323;
B 12 32 126,308;
B 20 4 132,262;
B 20 4 132,238;
B 8 12 134,304;
B 8 12 144,322;
B 4 56 142,264;
B 14 4 149,262;
B 4 34 146,305;
B 16 22 162,299;
B 8 8 158,282;
B 4 20 156,270;
B 8 6 158,287;
B 16 82 182,241;
B 8 8 184,164;
B 4 140 184,90;
B 4 8 188,164;
B 4 122 192,221;
L NI;
B 12 12 44,272;
B 12 12 58,238;
B 16 12 72,238;
B 12 12 70,262;
B 12 16 92,320;
B 12 16 108,320;
B 16 12 128,238;
B 12 12 130,262;
B 12 12 156,272;
L NP;
B 8 8 28,354;
B 4 22 26,339;
B 4 36 26,310;
B 24 4 38,294;
B 6 8 37,282;
B 42 4 57,226;
B 4 10 38,275;
B 4 46 38,249;
B 12 4 44,272;
B 8 6 48,245;
B 10 4 55,244;
B 4 12 58,238;
B 32 4 74,180;
B 4 38 60,201;
B 10 4 73,268;
B 10 4 73,244;
B 4 12 70,262;
B 4 12 70,238;
B 18 4 81,278;
B 4 40 74,308;
B 4 8 74,284;
B 4 30 76,211;
B 8 6 80,269;
B 8 6 80,243;
B 12 4 88,244;
B 8 8 90,288;
B 4 38 88,201;
B 88 4 132,180;
B 4 22 92,257;
B 4 12 92,274;
B 4 36 92,310;
B 4 4 92,180;
B 12 4 112,244;
B 8 8 110,224;
B 8 8 110,288;
B 4 22 108,257;
B 4 12 108,274;
B 4 36 108,310;
B 18 4 119,278;
B 4 32 112,208;
B 8 6 120,269;
B 8 6 120,243;
B 42 4 143,216;
B 10 4 127,268;
B 10 4 127,244;
B 4 24 124,204;
B 4 40 126,308;
B 4 8 126,284;
B 4 12 130,262;
B 4 12 130,238;
B 24 4 162,294;
B 12 4 156,272;
B 6 8 163,282;
B 4 10 162,275;
B 4 58 162,243;
B 8 8 172,340;
B 4 8 174,332;
B 4 36 174,310;
B 8 8 178,194;
B 6 8 179,164;
B 4 14 178,175;
B 6 4 185,196;
B 4 88 186,242;
L NC;
B 4 8 4,226;
B 4 8 4,160;
B 4 8 12,226;
B 4 8 12,160;
B 4 4 28,354;
B 4 4 30,224;
B 4 4 38,282;
B 4 8 38,304;
B 4 4 42,282;
B 4 4 48,240;
B 4 4 48,244;
B 4 8 50,30;
B 4 8 56,322;
B 4 8 66,304;
B 4 8 68,204;
B 4 4 78,340;
B 4 4 80,264;
B 4 4 80,268;
B 4 4 80,238;
B 4 4 80,242;
B 4 4 90,288;
B 4 8 96,204;
B 4 8 100,304;
B 4 8 100,322;
B 4 8 104,204;
B 4 4 110,224;
B 4 4 110,288;
B 4 4 120,264;
B 4 4 120,268;
B 4 4 120,238;
B 4 4 120,242;
B 4 4 122,354;
B 4 8 132,204;
B 4 8 134,304;
B 4 8 144,322;
B 4 4 158,282;
B 4 4 162,282;
B 4 8 162,304;
B 4 4 172,340;
B 4 4 178,194;
B 4 6 178,207;
B 4 8 178,276;
B 4 8 178,244;
B 8 4 182,164;
L NM;
B 200 16 100,8;
B 16 152 8,92;
B 16 108 8,274;
B 200 32 100,196;
B 14 12 17,322;
B 102 8 75,354;
B 80 12 64,304;
B 80 12 64,322;
B 88 8 70,224;
B 12 8 40,282;
B 8 12 48,242;
B 8 12 48,232;
B 108 108 100,106;
B 8 28 50,38;
B 102 8 125,340;
B 102 8 125,340;
B 8 12 80,266;
B 8 12 80,240;
B 10 6 89,269;
B 8 20 90,282;
B 78 12 135,304;
B 80 12 136,322;
B 10 6 111,269;
B 8 20 110,282;
B 8  12 120,266;
B 8 12 120,240;
B 8 14 144,351;
B 12 8 160,282;
B 8 98 178,261;
B 12 8 182,164;
L NG;
B 92 92 100,106;
DF;

(PadCap);
DS 777 125/1;
L NM;
B 200 16 100,8;
B 108 108 100,106;
L NG;
B 92 92 100,106;
DF;

(Rama glowna1);
DS 1001 125/1;
C 207 T 0 300;
C 777 R 0 -1 T
0,700;
C 777 R 0 -1 T
0,900;
C 777 R 0 -1 T
0,1100;
C 777 R 0 -1 T
0,2200;
C 777 R 0 -1 T
0,2400;
C 777 R 0 -1 T
0,2600;
C 206 R -1 0 T
600,2900;
C 777 R -1 0 T
800,2900;
C 777 R -1 0 T
1000,2900;
C 777 R -1 0 T
1200,2900;
C 777 R -1 0 T
1400,2900;
C 777 R -1 0 T
1600,2900;
C 777 R -1 0 T
1800,2900;
C 206 R 0 1 T
2100,2400;
C 204 R 0 1 T
2100,2200;
C 204 R 0 1 T
2100,2000;
C 209 R 0 1 T
2100,1800;
C 202 R 0 1 T
2100,900;
C 204 R 0 1 T
2100,700;
C 204 R 0 1 T
2100,500;
C 204 R 0 1 T
2100,300;
C 205 T 400,0;
C 205 T 600,0;
C 205 T 800,0;
C 205 T 1000,0;
C 205 T 1200,0;
C 205 T 1400,0;
C 207 R 0 1 T
1800,0;

L ND;
L NC;
L NM;
B 330 32 1755,196;
B 32 124 1904,242;
B 16 304 2092,152;
B 304 16 1948,8;
B 16 908
2092,1550;
B 32 908
1904,1550;
B 32 124
1904,2658;
B 124 32
1858,2704;
B 304 16
1948,2892;
B 16 304
2092,2748;
B 404 16 202,2892;
B 16 304 8 2748;
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B 32 124 196,2658;
B 224 32 292,2704;
B 16 908 8,1550;
B 32 908 196,1550;
B 16 304 8,152;
B 408 16 204,8;
B 40 2 60 2840;
B 2 40 60 2840;
B 40 2 2040 60;
B 2 40 2040 60;
DF;

(Butt);
DS 2 125/1;
L NM;
B 12 8 6,4;
L NC;
B 8 4 6,4;
L ND;
B 8 8 4,4;
L NP;
B 6 8 9,4;
DF;

(SubUklad1);
DS 1 125/1;
L NP;
B 4 364 1706,620;
B 132 4 1642,440;
B 4 104 1578,390;
L NM;
B 226 24 1289,312;
B 92 16 1570,422;
B 16 54 1608,403;
B 54 8 1709,380;
B 8 46 1734,361;
B 78 16 1563,308;
B 50 8 1707,304;
L NP;
B 20 4 1722,312;
B 4 38 1714,295;
B 296 4 1568,278;
B 4 36 1422,262;
B 26 4 1589,322;
B 4 40 1578,304;
B 360 4 1400,286;
B 4 44 1222,266;
B 382 4 1211,332;
B 4 90 1022,289;
B 56 4 1552,340;
B 4 278 1714,463;
B 34 4 1699,326;
L NM;
B 126 24 1463,426;
B 24 36 1430,366;
B 24 36 1484,360;
B 126 24 1463,312;
B 84 16 1642,384;
B 16 24 1620,344;
B 16 24 1656,340;
B 84 16 1642,308;
B 8 12 1740,322;
B 8 12 1758,320;
L NC;
B 4 8 1484,360;
B 4 4 1430,426;
B 4 8 1430,366;
B 4 4 1430,312;
B 4 8 1656,340;
B 4 4 1620,384;
B 4 8 1620,344;
B 4 4 1620,308;
B 4 8 1758,320;
B 4 4 1740,342;
B 4 8 1740,322;
B 4 4 1740,304;
L NP;
B 30 12 1511,336;
B 24 30 1484,345;
B 36 42 1430,387;
B 60 12 1430,336;
B 20 8 1674,324;
B 16 20 1656,330;
B 24 28 1620,358;
B 40 8 1620,324;
B 8 10 1758,315;
B 12 14 1740,329;
B 20 4 1740,312;
L NI;
B 30 60 1430,387;
B 20 40 1620,358;
B 10 20 1740,329;
L ND;
B 24 12 1460,366;
B 24 24 1484,366;
B 24 24 1430,426;
B 12 30 1430,399;
B 24 12 1430,378;
B 36 54 1430,345;
B 24 18 1430,309;
B 16 8 1640,344;
B 16 16 1656,344;
B 16 16 1620,384;
B 8 20 1620,366;
B 16 8 1620,352;
B 24 36 1620,330;
B 16 12 1620,306;
B 8 4 1750,322;
B 8 8 1758,322;
B 8 8 1740,342;
B 4 10 1740,333;
B 8 4 1740,326;
B 12 18 1740,315;
B 8 6 1740,303;
L NP;
B 4 2326 806,1457;
B 4 2384 814,1458;
L ND;
B 308 8 446,2350;
B 292 8 438,2150;
B 8 1708 596,1500;
B 8 1308 580,1500;
B 308 8 446,650;
B 292 8 438,850;
L NM;
B 8 2192
1376,1576;
B 8 2192
1424,1576;
B 488 8 510,2616;
C 2 T 412,238;
C 2 T 612,238;
L NP;
B 196 4 718,268;
B 390 4 613,296;
L NM;
B 1078 24 863,426;
B 24 426 336,225;
B 142 8 229,650;
L ND;
B 4 30 414,225;
B 4 30 614,225;
B 4 30 814,225;
B 4 30 1014,225;
C 2 T 1012,238;
L NC;
B 4 4 296,650;
L NP;
B 4 2446 822,1467;
L ND;
B 4 30 1214,225;
B 4 30 1414,225;
L NM;
B 24 114 1188,267;
C 2 T 1212,238;
C 2 T 1412,238;
L NM;
B 42 8 1751,304;
L NP;
B 10 4 1767,312;
B 30 4 1785,312;
B 4 92 1798,356;
L NM;
B 42 8 1751,342;
L NP;
B 100 4 1762,600;
B 108 4 1758,800;
B 72 4 1776,2300;
B 60 4 1782,2100;
L NM;
B 14 8 1749,1944;
B 14 4 1737,1912;
B 4 386 1732,2103;
B 4 150 1744,2021;
C 2 T 1742,2094;
C 2 T 1730,2294;
L NM;
B 8 78 1150,2703;
B 234 8 1263,2668;
B 8 78 1650,2703;
B 234 8 1537,2668;
B 50 8 1429,2684;
B 8 62 1450,2711;
B 8 62 1350,2711;
B 50 8 1371,2684;
B 8 100 746,2692;
B 8 60 850,2712;
B 42 8 833,2686;
C 2 T 742,2642;
C 2 T 742,2612;
L NP;
B 56 4 780,2618;
B 64 4 784,2648;
C 2 T 812,2682;
L NM;
B 118 8 215,2550;
B 8 74 270,2583;
B 142 8 229,2350;
B 142 8 229,2150;
L NC;
B 4 4 296,2350;
B 4 4 296,2150;
L NP;
B 16 4 1804,400;
DF;

(SubUklad2);
DS 3 125/1;
L NP;
B 4 54 420,271;
B 4 26 622,257;
C 2 T 812,238;
L NM;
B 142 8 229,850;
L NC;
B 4 4 296,850;
L NM;
B 8 2208
1392,1584;
B 8 2208
1408,1584;
DF;

(ST2_StrukturaTest
owa2);
DS 1002 125/1;
C 1001 T 0,0;
C 1 T 0,0;
C 3 T 0,0;
DF;
C 1002 T 0,0;
E
```

6.1.2. Format Translators

The open systems and turnkey systems [CADE93, Gajs88, Tann96a-b, Smit97, WeEs93] are the two main considerations for CAE software development in VLSI CAD tools. System performance, utility features and elasticity depends on software structures, systems tasks, programming tools and their cooperation possibility.

For the integration of different tools in one, newly problem-oriented system, the cooperation problem is a very decisive one. In ASIC/DI Program for ST2 and AF4 test structures design, we chose a software solution for a part of an open CAD system applicable to VLSI structure design, work out bidirectional translators for graphic editor using DXF (Drawing eXchange Format) format in describing VLSI structures and widely used in Silicon Foundry (parallel with GDSII) format CIF (Caltech Intermediate Form) used for the same task [PaZn94].

The call command for both translators has a following form:

cif2dxf [-[b][n][l][lambda]] inputfile [outputfile],
dxf2cif [-[b][n][l][lambda]] inputfile [outputfile].

cif2dxf converts CIF to the DXF files, dxf2cif inversely. Parameters in brackets are optional, when omitted, translators use default values.

Parameter b specifies that during processing the structure of CIF symbols or DXF blocks (accordingly to the translator) will be saved, default is exploding of these elements.

Parameter n tells to keep the sequence of elements from input file, default is sorting in accordance with layers inside symbols or blocks.

Parameters l and lambda specify the value of technological coefficient λ, default is λ=2.5μm.

inputfile is the full path with input file name.

outputfile is optional full path with output file name.

Translators are forcing the extension of files as ".cif" and ".dxf" respectively. In case when a file with the same name exists, translators automatically make a backup copy of the file and give ".bak" extension. When a translation process takes place, translators create the report file (extension ".rpt") which can be used for fast errors detection in the input file.

6.1.3. VLSI Libraries

The designs of ST2 and AF4 structures are based on tested, working cell library STDCELL1 ver. 1.0 [L. Znamirowski: "Computer-Aided Design of VLSI Structures", Laboratory 5 Manual, CAE Laboratory, Institute of Informatics, Silesian University of Technology, Gliwice 1988 (in Polish), Znam03b, Znam93b, NeMa83]. Selected cells from this library (nMOS process, λ=2.5μm) are presented in Fig. 6.1.

The contact pads PadCap and PadGnd are used in dielectric absorption measurements as an interface between metal interconnects on a chip, and wires of package. PadIn4 and PadOut4 cells are used for connection of the scaled inverters (cells: Inverter, Inverter1, Inverter2) to the circuitry of the package. These inverters are used for determination of switching speed in dependency on dimension scaling.

In Fig. 6.2, are presented selected elements from CMOS LOCOS ver. 2.0 library (λ=1.5μm). Elements 1000, 1130, 1220, and 1410 are modular logic gates, cells 9530, 9250, 9670 are bonding pads [L. Znamirowski, M. Skrzewski, R. Pawlowski, S. Warecki: "CAD Sys-

tems for VLSI Design", Research Report BK-17/Rau2/94, Institute of Informatics, Silesian University of Technology, Gliwice 1994 (in Polish), Znam03b, Hein88]. In the upper left corner is the cell inv_min used for comparative study of switching transients between gates, when the dielectric absorption phenomenon is taken into consideration (p. 2.8). The CIF description of inv_min cell has the following form:

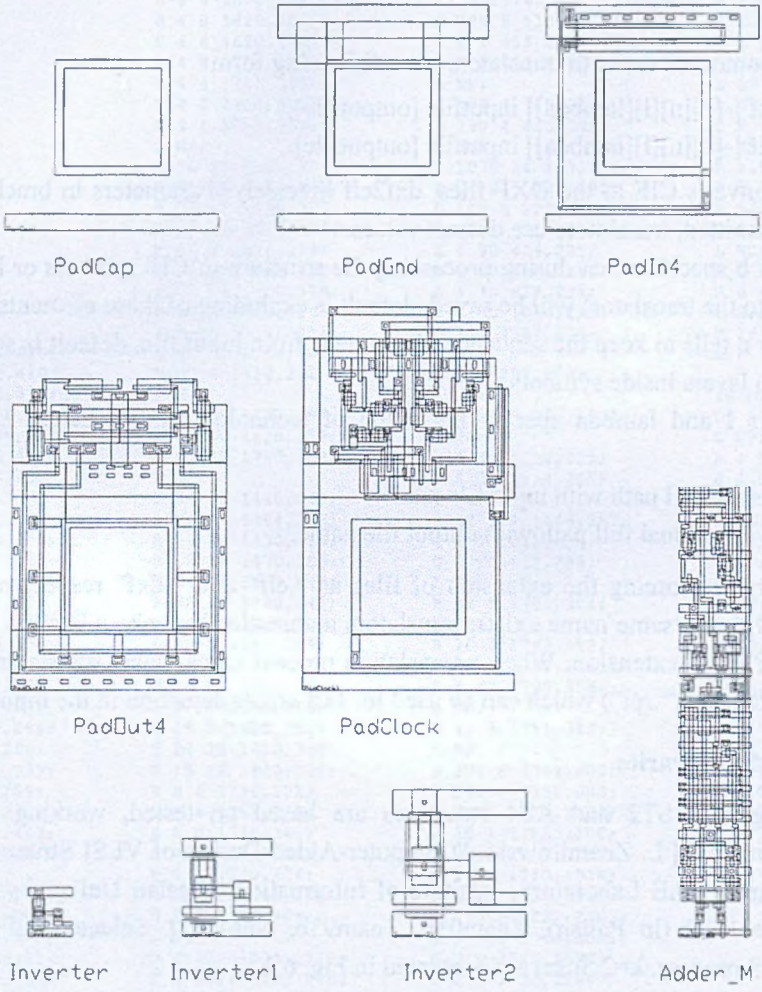


Fig. 6.1. Selected elements from STDCELL1 ver. 1.0 library
Rys. 6.1. Wybrane elementy z biblioteki STDCELL1 ver. 1.0

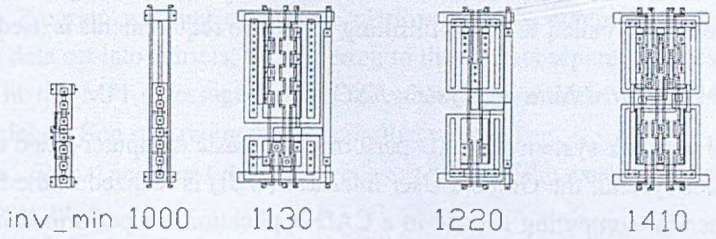
```
DS 1 75/1;
9 INV_MIN;
L PWE;
B 24 68 20,34;
L NWE;
B 24 68 20,120;
L POA;
B 12 12 20,122;
B 8 12 20,110;
B 12 12 20,98;
B 12 12 20,12;
L NOA;
B 12 12 20,142;
B 12 12 20,56;
B 8 12 20,44;
B 12 12 20,32;
L POLY;
B 4 4 6,90;
B 12 12 20,74;
B 10 4 31,74;
B 4 4 2,74;
B 18 4 19,110;
B 4 24 8,100;
B 4 32 6,72;
B 4 14 8,53;
B 22 4 17,44;
L CONT;
B 4 4 20,142;
```

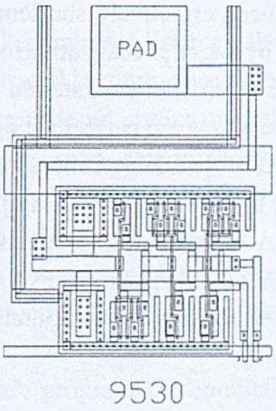
```
B 4 4 20,122;
B 4 4 20,98;
B 4 4 20,74;
B 4 4 20,56;
B 4 4 20,32;
B 4 4 20,12;
L MET1;
B 6 2 20,67;
```

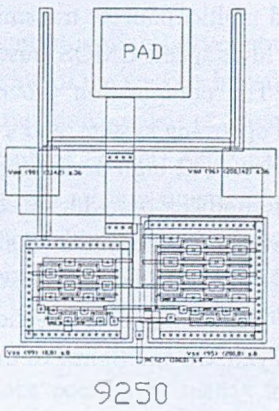
```
B 12 2 20,137;
B 6 8 20,132;
B 12 12 20,122;
B 12 36 20,86;
B 6 4 20,64;
B 12 12 20,56;
B 12 12 20,32;
B 6 8 20,22;
```

```
B 12 2 20,17;
B 36 16 18,146;
B 36 16 18,8;
L VIA;
B 4 4 20,86;
L MET2;
B 14 10 7,86;
B 12 12 20,86;
```

```
L PVX;
L SCH;
DF;
C 1 T 0,0;
E
```







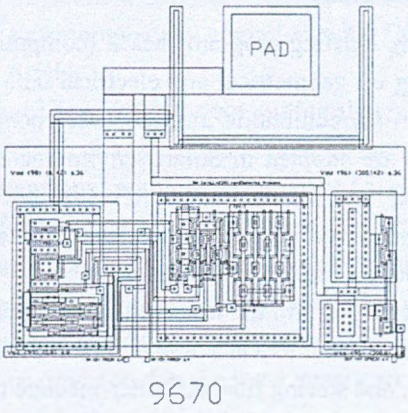


Fig. 6.2. Selected elements from CMOS LOCOS ver. 2.0 library
Rys. 6.2. Wybrane elementy z biblioteki CMOS LOCOS ver. 2.0

6.2. Appendix II – Interconnections Measurements

6.2.1. Supercomputing in VLSI Interconnections Computations

The computer algorithms used for MTL characterization for design purposes (p. 2.6.3) are complex and time-consuming so the effective use of CAD tools needs a proper configuration of computing resources. For these tasks, the workstation/supercomputer (parallel computer) system [Sewe00, SePZ01] called KSCAD fulfilling the above requirements is used.

Outline of the Integrated Network System KSCAD

The integrated network system KSCAD performs two basic computer-aided design tasks in the two-computer system: the Graphic User Interface (GUI) is realized in the PC workstation, and the numerical computing needed in a CAD application are performed in the multiprocessor based parallel computer. Time-consuming computations of energy characterization of the scaled multiconductor transmission lines has been effectively shortened and the optimization of high speed CMOS buses was possible by parallel realization of the numerical procedures. The computation process is controlled from the workstation working under Win98/2000 operating system, and a numerical computations are performed by the Sun Enterprise 6500 server (12 high performance, 64-bit SPARC™ [Scalable Processor ARChitecture] V9 RISC microprocessors with full throughput equal to 6 GFLOPS) working under the Solaris™ 7 Operating Environment [SunE00]. The KSCAD system integrates six main software modules distributed between a supercomputer (modules AlfaU, SerwerU, MM2, and SCALING2 characterized later) and a workstation working as a computation control unit (modules: Wykres3d and Spline of the KSCAD system).

Tasks Performed in the System

In the KSCAD system, existing programs MM2 (computing the capacitance coefficients matrix of the MTL basing on geometrical and electrical data from the layout of a structure) and SCALING2 (program for computing a quasi-static energy gathered in electrostatic and magnetic fields of MTL) are adopted in Solaris environment, broken into the separate processes, executed in parallel, and finally, integrated results are sent to the workstation for presentation in graphical or numerical form. These tasks are performed by communication protocols and the AlfaU module residing on a Sun computer.

The modules of a system perform the tasks of data preparation, inter-module communication, network communication, numerical computing for CAD with inter-processes communication control, graphics, and storing final and inter-mediate results on systems' disks.

Software Tools

Completion of the system required adoption of existing stand alone CAD programs and writing a few new modules for system integration. Depending on proper platform [Micr98,

Stev95], it was necessary to use different compilers, scripts, protocols etc. In a system we have six main modules:

Wykres3d - Control program in the KSCAD system maintaining the main menu in the workstation, organizing operation on the input and output data in the computing process, and responsible for communication between operating systems in the two-computer CAD system. Wykres3d module resides on PC workstation – compiled in Visual C++ environment.

AlfaU - Program working on a Unix platform. AlfaU organizes computing process by division the data set into subsets, and ordering to the subsets separate processes. This function is fulfilled in the MPI (Message-Passing Interface) environment [GrLS94, Usin00]. AlfaU module resides on Sun supercomputer – compiled with `mpicc`.

Compilation: `/usr/local/mpi/bin/mpicc -o` <name of the executable program> <name of the source program>.

Execution: `/usr/local/mpi/bin/mpirun -np` <number of processes> <name of the executable program>.

SerwerU - Program for listening the demands of client in a client-server communication model. In the SerwerU program are used the system function of the sockets interface [Fost95]. Before starting any input/output operation, the system function `socket()` have to be used. System function `bind()` determined the name for non-name socket. After call a function `socket()`, client process adds a socket descriptor calling the system function `connect()` to set a connection with server. Function `listen()` declares readiness for connection receiving, next connection server can complete the system function accept(), to fulfill a request of the waiting client process. SerwerU module resides on Sun supercomputer – compiled with CC compiler.

MM2 - Batch program for computing the capacitance coefficient matrix for multiconductor transmission line basing on geometrical and electrical data of the structure [Kowa91]. MM2 module resides on Sun supercomputer – compiled with CC compiler. This is done while working under control of AlfaU.

SCALING2 - Batch program [Znam98b] for computing the energies for multiconductor transmission line basing on geometrical and electrical data of the structure. SCALING2 can use scaling factors in three dimensions: width of conductors (α_1 scale factor in logarithmic scale denoted as alfa1), high of conductors (α_2 scale factor – in logarithmic scale alfa2), and distance between conductors (α_3 - alfa3). SCALING2 computes the following partial results (for convenient processing in next applications basing on KSCAD system):

- electrostatic energy of the capacitance part of the "slice",
- static magnetic field energy stored in the inductance part of the "slice",
- energy dissipated on conductors' resistance,
- conservative energy (for capacitance and inductance of the "slice"),
- total energy.

SCALING2 module resides on Sun supercomputer – compiled with f77 compiler. Working under control of AlfaU module.

Spline - Program for interpolation using spline technique [VanZ00]. Spline module resides on PC workstation – compiled in Visual C++ environment.

Client-Server Communication Model

In the computer network applications, the standard model of data exchange is a client-server communication model. Server is a process waiting for requirement to connect from process called client to fulfill the determined tasks.

In KSCAD system the selected communication protocol is TCP/IP. Firstly, the layer TCP (Transmission Control Protocol) is responsible for correct delivery of data between client and server. In a case when data is lost, TCP initializes the retransmission until the data is completely and correctly received. This improve reliability of CAD system (in a case of time-consuming computation lost of data is expensive). Secondly, login to the supercomputer can be performed from arbitrary computer working in the Internet. In KSCAD system, the client workstation and computational server working in the network, communicate with each other using the package of subroutines that provide access to TCP/IP i.e. sockets interface [Fost95].

It was practical to implement character protocol for data exchange between network client and network server for interpretation of client requests and to inform client for which request the answer is valid. The features of a character protocol are following:

begin 'p' - start of data sending and start of computing (Fig. 6.4)
status 's' - status of computing presenting error type or computations progress
end'k' - end of data transfer
purge 'n' - time-break of computations
error 'b' - error during session
resume'w' - transfer of results (Fig. 6.4)
results 'z', 'j', 'd', 't', 'c' - transfer of computed energies (p. 2.6.1): electrostatic, magnetic, dissipated, conservative, and a total respectively.

Parallel Computations

To speed up time consuming computations, in the system KSCAD, a supercomputer with 12 processors was used. The computations in multiprocessor's system are comparable to computations performed with parallel computations on multicomputer's system. In both cases the programs have to communicate with each other, and one process (or respectively program) have to supervise all operations. The difference is only in the type of communication. In multicomputer system, messages are sent through the computer network. In a case of multiprocessor system, the queues of messages resulting from processes' activity are created and supervisor process gather the waiting results together. The operating system of multiprocessor

computer have to fulfill these requirements. The Solaris 7 Operating Environment is very well adapted to the tasks of this kind.

For the parallel computations, the numerical task of CAD for VLSI MTL energy characterization performed in the KSCAD system, have to be moved from sequential to the parallel execution. In our case, the massive computation for vector scaling of MTL are based on a declared grid which determine a set of scale vectors (p. 2.6.3). Division of this set of scale vectors into 11 similar subsets is assumed, and indicate last processor (twelve) as a master gathering results. Each parallel process is ordered to the physical processor and the processes are mutually independent. Also, all variables in the processes are unique in each module. Data are gathered on a disk, and can be simultaneously read by processes. The parallel process of computing in the KSCAD system is coded using MPI Environment by a program module AlfaU. Message-Passing Interface is a specification for a library of routines to be called from ANSI C and Fortran 77 programs.

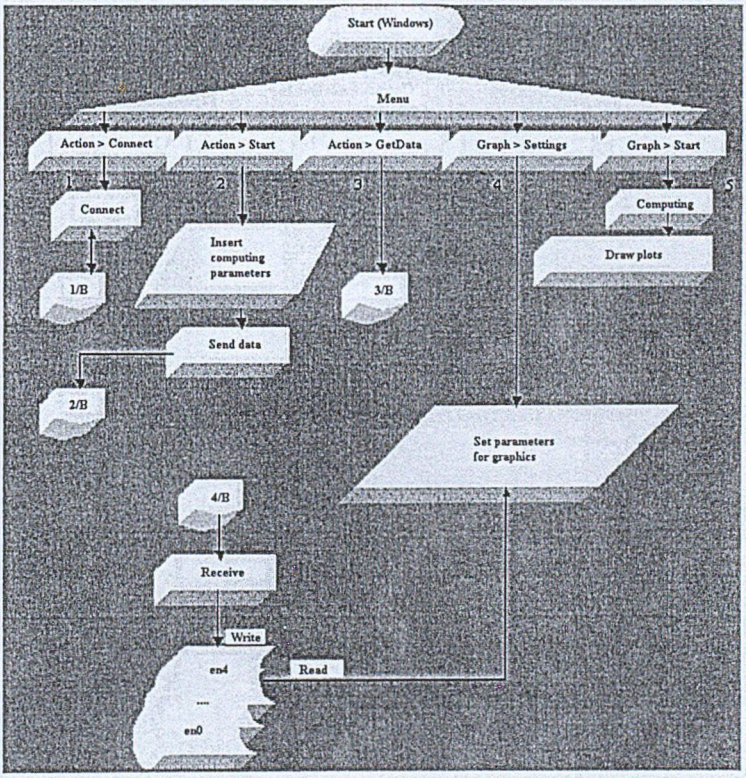


Fig. 6.3. Flow graph of the system: Part A - Data flow for Win98/2000 workstation
Rys. 6.3. Schemat blokowy przepływu danych dla stacji Win98/2000

Sending and receiving of messages between the parallel processes is basic operation in MPI environment for fulfilling the communication tasks. The basic point-to-point communi-

cation operations are *send* and *receive* implemented by the MPI functions `MPI_Send()` and `MPI_Recv()`, with proper (slightly different for the languages Fortran 77 and ANSI C, but functionally analogous) sets of arguments. In the system KSCAD, the C code of the modul AlfaU is divided into three parts, a common part for master and slave processes preparing data gotten from GUI (PC workstation), a second part for 11 slave processes sending the results (`MPI_Send()` function) for energies computing (the main part of time-consuming computation), and third part for master gathering results from 11 slave processes (`MPI_Recv()` function). The second and third part are surrounded with MPI environment activation functions `MPI_Init()` and `MPI_Finalize()`, the functions `MPI_Comm_rank()` and `MPI_Comm_size()` are used for processes initialization and find out the number of processes. The internal inter-process' communication in AlfaU module is based on `MPI_DOUBLE` C datatype and `MPI_COMM_WORLD` predefined communicator [GrLS94, Sewe00].

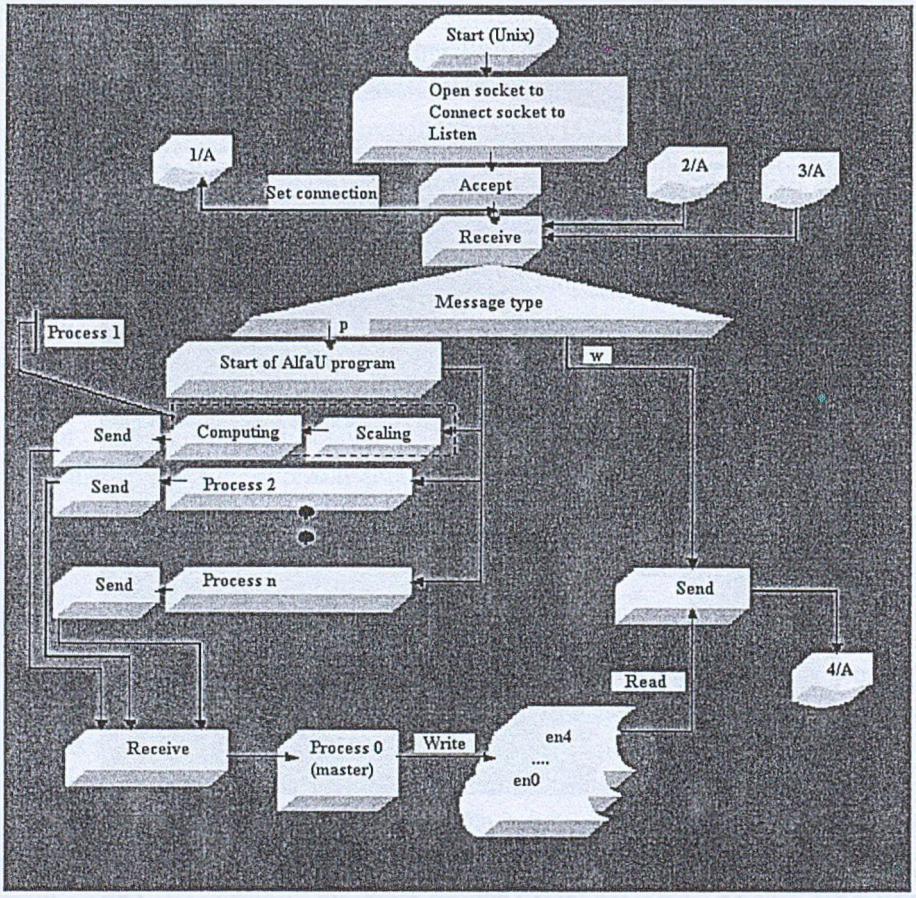


Fig. 6.4. Flow graph of the system: Part B - Data flow for Sun Enterprise 6500
Rys. 6.4. Schemat blokowy przepływu danych dla superkomputera Sun Enterprise 6500

GUI of the KSCAD System

Graphic User Interface in the KSCAD system is running on PC workstation as a control program Wykres3d. Control program maintains the main menu in the workstation, organizes operations on the input data and output data from the computing process. The output data have two form: the results 2D tables (scale factors alfa2 and alfa3) with alfa1 as a parameter, and a visualized plots. The quasi-3D plots are performed basing on 2D tables and the spline interpolation [FDFH95, Pavl87]:

alfa1 – consecutive plots (width of conductors),

alfa2 – x axis (high of conductors),

alfa3 – y axis (distance between conductors), and energies – z axis (Figs. 2.28 – 2.31).

Flow Algorithm of the System

The KSCAD system integrates six program modules: three existing were adopted and modified for requirements of the system [Znam98b, Kowa91, VanZ00], and three were work out as new [Sewe00].

Flow algorithm of the system is presented in Figs. 6.3 to 6.5.

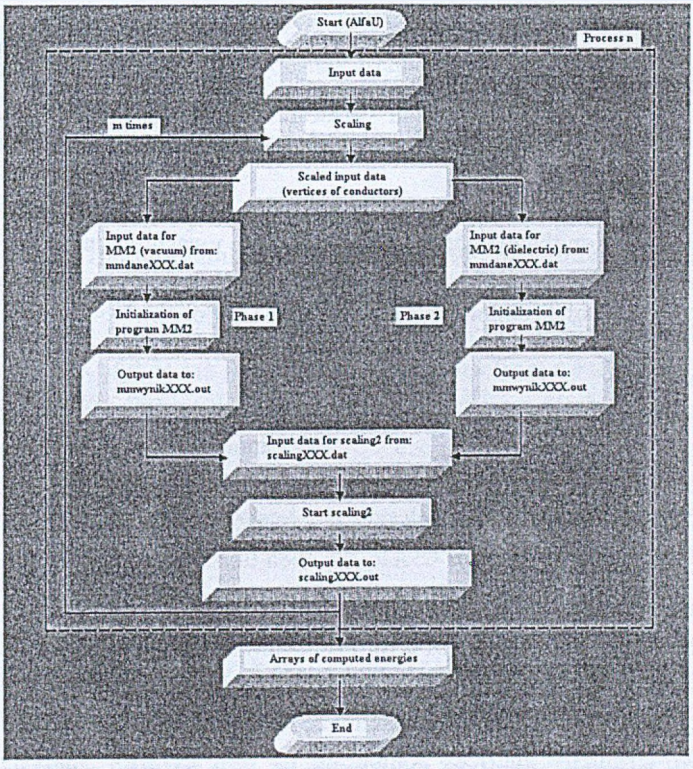


Fig. 6.5. Data flow performed by n^{th} process

Rys. 6.5. Schemat blokowy przepływu danych w n-tym procesie

Data flow for Win98/2000 workstation (part A) is presented in Fig. 6.3. The connections between parts A and B describe the pairs of contacts e.g. 1/B-1/A. The part B of the system characterizing data flow for Sun Enterprise 6500 is presented in Fig. 6.4. After start of AlfaU program, eleven processes in parallel, solving the CAD tasks, and twelfth process gathers the results on a disk, and put them to the PC workstation for presentation. The user can get result which are basic for design, but it is also possible to access the intermediate results of computation. This is necessary for checking the correctness of actual algorithms as well as in future development of the system.

In Fig. 6.5, more detailed the data flow in one of eleven processes is presented. Phase 1 and phase 2 represent solving the equations (2.65) and (2.68), as an input to the second part of computing in a n^{th} process branch.

6.2.2. Selected Software Supporting the Interconnections Measurements

1. Program TT-MAX-A/ACCURACY

Program for computation of the Maxwell matrix in [pF/cm] from a two-terminal capacitance matrix in [pF], for a segment of the line with a given length in [um]. Subroutine ACCURACY computes the relative and absolute errors in the Maxwell's matrix computing.

L. Znamirowski: "Silicon Compilation and its Implementation on the Workstations", Research Report, Institute of Informatics, Silesian University of Technology, BK-245/RAu2/1999, Gliwice 1999 (in Polish).

L. Znamirowski, "CAD for VLSI Design", Research Report, Institute of Informatics, Silesian University of Technology, Research Report BK-210/RAu2/2000, Gliwice 2000 (in Polish).

2. Program DIELEK

Program for computation the dielectric parameters from measurements.

L. Znamirowski: "dielek.for an Identification Program", Institute of Informatics internal report, Silesian University of Technology, Gliwice 1994 (in Polish).

3. Program SCALING

Program for computation the total energy of multiconductor transmission lines (new version SCALING2).

L. Znamirowski: "Coupled Multiconductor Interconnections in VLSI/ULSI Structures", Institute of Informatics internal report, Silesian University of Technology, Gliwice 1994 (in Polish).

4. Program ACC99

Program for the numerical analysis of error propagation in computing the Maxwell matrix and "two-terminal" matrix of the multiconductor structure from measurement vector M (indirect measurement). Program is based on capacitance measurements method and algorithm for Maxwell and "two-terminal" matrices computing as well as error analysis described in [ZnPa98b].

6.3. Appendix III – Reprogrammable FPAA Structures

6.3.1. FPAA Matrices

A field programmable analog array, built in CMOS technology [Moto97a, Anad01b], contains uncommitted operational amplifiers, switches, and banks of programmable switched capacitors (SC). The chip is divided into 20 identical, configurable analog blocks (CABs), each composed of an operational amplifier, five capacitor banks, and switches that can be used to interconnect the cell components and determine their operation. There are both static and dynamic CMOS switches. The static switches are used to determine the configuration of cell components and inter-cell connections. These switch settings are determined once during the programming phase of an application after which they remain unchanged. The dynamic switches are associated with capacitors and are switched periodically during the circuit operation changing the effective function of capacitors as typically exploited in SC circuits (Fig. 6.12). Both static and dynamic switches are electronically controlled and thus the functionality of each CAB, the capacitor sizes, and the interconnections between CABs are programmable. As a result many diverse circuit architectures can be implemented and used in the adaptive filtering and control, predictive control, adaptive DSP front-end, adaptive industrial control and automation, intelligent sensors, dynamic recalibration of remote systems, conditioning of analog signals including ultra-low frequency signal conditioning, signal generation as well as a large number of others analog applications. Generally, the parameters of a given application performed by the configured FPAA chip, are functions of the capacitor values and internal connections.

The FPAAs used in this study are Motorola's MPAA020 and AN10E40 whose contain 41 operational amplifiers, 100 programmable capacitors, 6864 electronic switches arranged into the 20 CABs, and 13 input/output buffers. The array is structured in a grid that contains the 20 CABs arranged in a 4x5 matrix. Configuring an analog design within the array is performed by downloading 6K bits of data via RS232 communications from a PC or EPROM [Moto97c] and in case of AN10E40 additionally from four flash memories. Both chips can be initialized on power up via an off FPAA chip memory.

The data stream contains information to configure the individual cells, the cell to cell interconnections, internal voltage reference as well as the input and output connections. During the configuration download process all cells are placed in a power-down mode to protect the CABs against undesirable high currents. The switches allow control over the circuit connectivity and capacitor values in addition to other features.

The complexity of control is so high that a supporting software was developed to facilitate the chip programming. The software allows a user to easily manipulate these field-programmable switches in order to implement a specific circuit. The chips programming software is called EasyAnalog™ [Moto97b] and AnadigmDesigner™ [Anad01a] and runs under Windows operating systems. General view of the FPAA chip configured by a computer, logic system or

memory is presented in Fig. 6.6a. Symbol T_p describes the time interval (Fig. 6.6b) of downloading the FPAA.

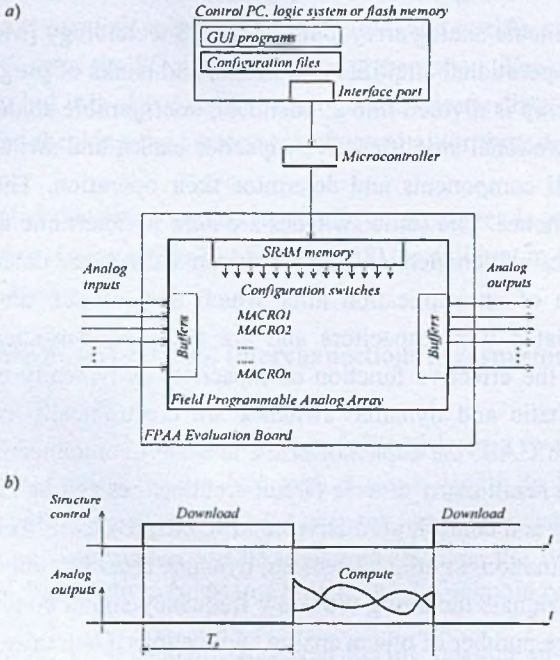


Fig. 6.6. General view of a controlled FPAA: a) structure, b) time dependencies
Rys. 6.6. Widok ogólny sterowanego układu FPAA: a) struktura, b) zależności czasowe

The basic interface window of EasyAnalog (AnadigmDesigner) displays (Fig. 6.7) a simplified view of 20 CABs, 13 I/O isolation amplifiers, programmable voltage reference, and inter-cell connecting lines. With a "point and click" action the user can select and place "macros" from a system function library (or own library, created by user) onto the chip in any feasible cell location. Routing between CAB's is performed by "Draw wires" graphic command. The external outputs from MPAA020 chip are connected to the pin bars placed around the FPAA package on the Evaluation Editing Board [Moto97c]. External input pin and external output pins are accessible by EasyAnalog software of the CAB.

Each system macro (from the system function library) is a pre-configured sub-circuit such as a gain-stages, different kind of filters, half and full-wave rectifiers, integrators, limiters, sample and hold elements voltage sources, just to mention some examples. Several macros can be placed onto the chip and "wired" together as required by an application. There are also some "pre-wired" application circuits, stored in a library, which can be selected and placed on the chip. Parameters of the library components can be selected and changed, as needed in the application, using pull-down menus and pop-up windows [Birk98, PGAA98]. The system function library is under continuous development [Moto97b, Anad01d].

Creation of the user-own library including specialized macros through the edition of reprogrammable structures (CAB cells editions – p. 6.3.2) is necessary for important extension of FPAA functions [Znam98a, ZnPV04,].

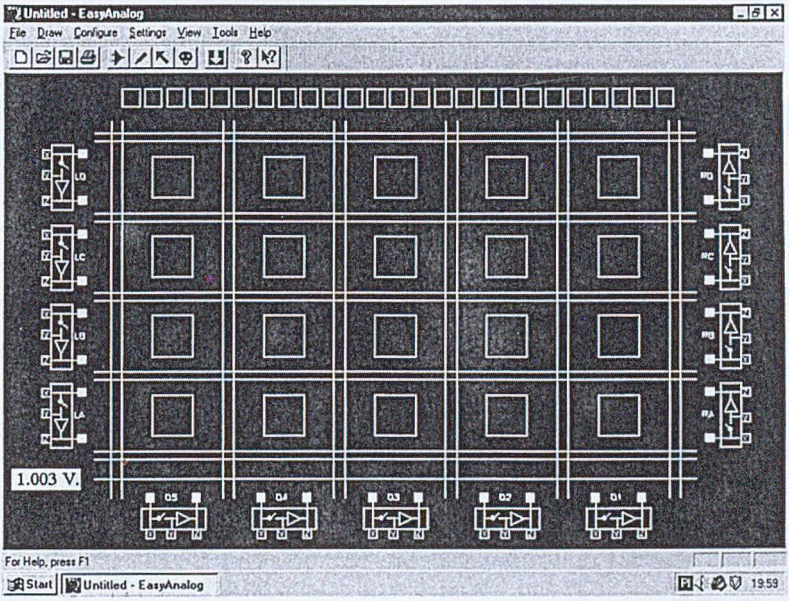


Fig. 6.7. Main menu and a "cross-bar" of the EasyAnalog GUI supporting FPAA programming

Rys. 6.7. Menu główne i „tablica łączeń" (interfejs graficzny) programu EasyAnalog wspomagające programowanie FPAA

Integration of mixed-mode functions in one chip, allowed for announcing so called the second generation FPAA family, Anadigmvortex, from Anadigm accessible probably in 2003. Compared with the first generation (MPAA020 and AN10E40), the most advanced member of this family (AN221E04) will consist of a 2x2 matrices of CABs surrounded by a fabric of programmable interconnect resources, its architecture will provide a significantly improved signal-to-noise ratio as well as higher bandwidth. This device also, will accommodate nonlinear functions such as sensor response linearization and arbitrary waveform synthesis. In addition, the AN221E04 chip will allow designers to implement an integrated 8-bit analog-to-digital converter on the FPAA using one of the dedicated output cells, eliminating the potential need for an external converter [Anad02a, Anad03a, Anad02b, Anad03b].

6.3.2. Edition of Reprogrammable FPAA Structures

Internal CAB cell structure is presented in Fig. 6.8. Routing between internal elements and wires inside of the CAB is performed by activation of the existing elements (Point and click command).

Editing the internal connections of the CAB it is possible to construct non-standard (not available in EasyAnalog library) one or multi CAB functions called macros. The array used for creation of macro is structured in a grid that contains the 20 CABs arranged in a 4x5 matrix (comp. Fig. 6.11). Created macros are placed in the user-defined library.

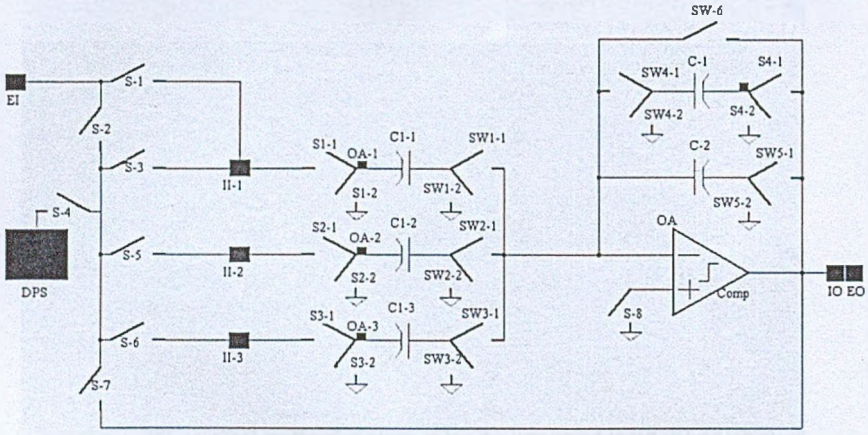


Fig. 6.8. Electrical diagram of the one Configurable Analog Block (CAB) cell: EI – external input, IO – internal output, EO – external output, S-1 to S-8 – static switches, S*i*-1(S*i*-2) and SW*j*-1(SW*j*-2) static or dynamic switches, DPS – Dynamic Phase Swapping or stopping waveform generator, II-*k* - internal inputs, OA-*k* – pins for connection to the +/– inputs of amplifier, C-1, C-2, C1-*k* – banks of capacitors, OA/Comp – operational amplifier

Rys. 6.8. Schemat konfigurowalnej komórki analogowej CAB: EI – wejście zewnętrzne, IO – wyjście wewnętrzne, EO – wyjście zewnętrzne, S-1 do S-8 – klucze statyczne, S*i*-1(S*i*-2) oraz SW*j*-1(SW*j*-2) klucze statyczne lub dynamiczne, DPS – formowanie sygnału generatora, II-*k* – wejścia wewnętrzne, OA-*k* – końcówki połączeniowe wejść +/– wzmacniacza operacyjnego, C-1, C-2, C1-*k* – banki kondensatorów, OA/Comp – wzmacniacz operacyjny

Fig. 6.9 presents windows used for the specification of modes of the static and programmable switches, using additional waveform generator for realization same standard (or specific) macros (DPS). Set of these waveform [Moto97b] is based on two basic non-overlapping waveforms ϕ_1 and ϕ_2.

Figs. 6.10 and 6.11 show the dialog box and environment of CAB around the central CAB for fixing the inter cell connections. All accessible points from current cell (the wire can be between internal cell input and output [internal output are not visible to the EasyAnalog Editor]) have the following locations:

LL– connection possible (II-*k*, Fig. 6.8) from the cell two cells to the left of the current cell.

UL– connection possible from the cell to the upper-left of the current cell. This is the only location for external input (when the external input is selected, UL is default).

U – connection possible from the cell above the current cell.
UR– connection possible from the cell to the upper-right of the current cell.
DL– connection possible from the cell down and to the left of the current cell.
D – connection possible from the cell directly below the current cell.
DR– connection possible from the cell down and to the right of the current cell.
L – connection possible from the cell to the left of the current cell.
R – connection possible from the cell to the right of the current cell.

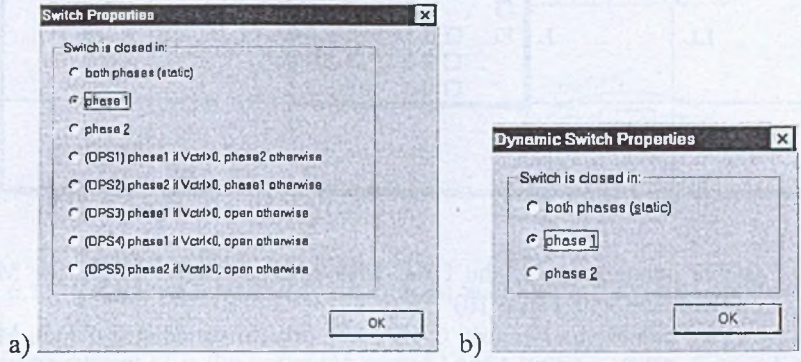


Fig. 6.9. Specification of modes of the S*i*-1 (S*i*-2) (a), and SW*j*-1 (SW*j*-2) (b) switches (*i*=1, ... 4, *j*=1, ... 5)
Rys. 6.9. Specyfikacja stanów grupy kluczy S*i*-1 (S*i*-2) (a), oraz grupy kluczy SW*j*-1 (SW*j*-2) (b) (*i*=1, ... 4, *j*=1, ... 5)

Constructing a macro, user has to be aware of possible processing errors which can occur when the parameters of capacitors and declared sub-frequencies (Figs. 6.12 and 6.13) are improperly chosen.

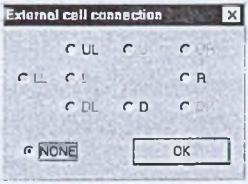


Fig. 6.10. External cell connection for II-1 – II-3 pins of the internal inputs of CAB
Rys. 6.10. Zewnętrzne połączenia wejść wewnętrznych II-1 – II-3 komórki CAB

Fig. 6.12 presents a window for manipulating the macro's parameters. The window is self-explanatory, only "use Clock" in a bottom of the "Set Macro Parameters" window needs an explanation given below.

The standard Master Clock Frequency (1MHz) is built-in into the Evaluation Board. To extend the functional flexibility of a macro and to allow accuracy optimization, four different

sub-frequencies can be chosen to built a macro. Each of them may be 1, 1/2, 1/4, 1/6, 1/8, ... , 1/62 of master clock frequency.

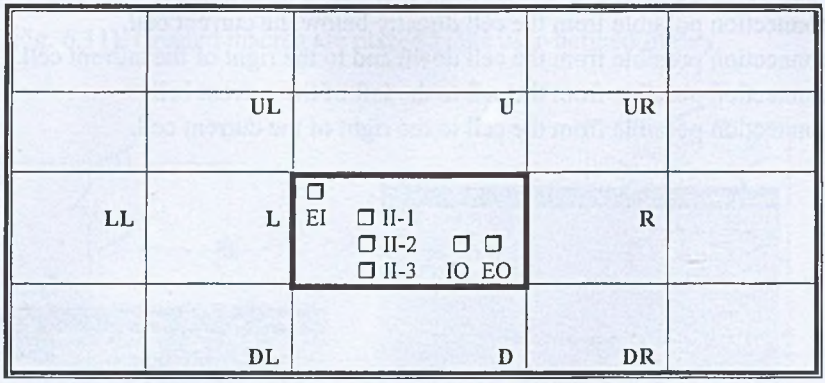


Fig. 6.11. Possible connections of the CAB with external CABs inside the MPAA020 chip (compare with Fig. 6.10)
Rys. 6.11. Możliwe połączenia komórki CAB z komórkami sąsiednimi układu MPAA020 (por. rys. 6.10)

This makes possible proper selection of relative values of resistances and capacitances in a feedback structures.

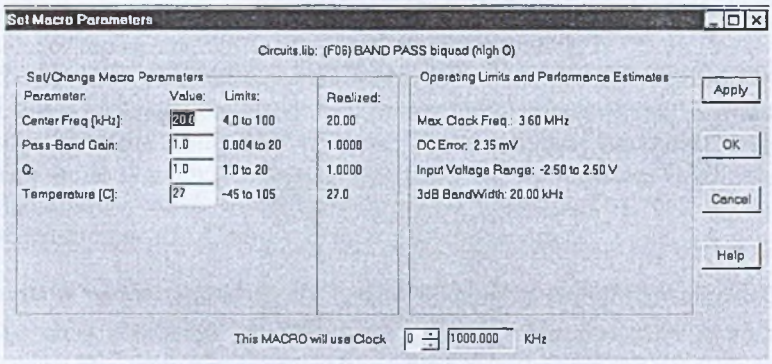


Fig. 6.12. Standard macro (F06) dialog box (schematic in Fig. 3.37) from Macro Libraries [Moto97b, Anad01d]
Rys. 6.12. Okno dialogowe standardowego makra (F06) (por. rys. 3.37) Biblioteki Makrostruktur [Moto97b, Anad01d]

The "SC resistance" in fact (Eq. (6.1)) depends on working capacitance and frequency of switching. From Fig. 6.13 we have:

for ϕ_1 = H; $Q_1=CV_1$,
and for ϕ_2 = H; $Q_2=CV_2$.

The charge transferred through equivalent resistor is described by equation:

$$\Delta Q = Q_1 - Q_2 = C(V_1 - V_2).$$

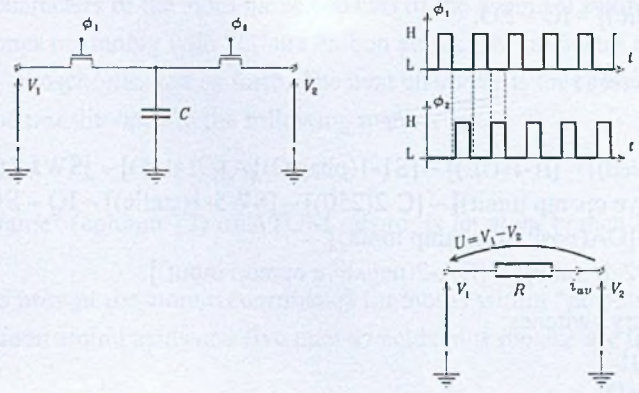


Fig. 6.13. Resistor in SC technology
Rys. 6.13. Realizacja rezystora w technologii SC (przełączanych pojemności)

The average current (T is the switching period) has a form:

$$i_{av} = \frac{1}{T}\Delta Q = \frac{V_1 - V_2}{\frac{T}{C}},$$

so the equivalent resistor (with sufficient assumptions):

$$R = \frac{T}{C} = \frac{1}{Cf_c}, \tag{6.1}$$

where f_c=1/T is the frequency of switching.

The set of available switching frequencies f_c is (1MHz, ... , 16.667, 16.129kHz), which allows for proper (and accurate) preparation of the macros.

The strong advantage of the FPAA is its capacity of on-the-fly reconfiguration and potential to implement different device or parameter settings [ZnPR02, ZnPV04, PVZH01]. For this reason the chip is so suitable for dynamic reconfiguration as it is demonstrated in the experimental investigations presented in this work.

6.3.3. Macro "Intgrp1"

Two-cell macro "Intgrp1" is placed in the upper-left corner of the CAB array.

We use the following notation (Fig. 6.8) to describe the structure of the macro:

phase1 – corresponds to the waveform ϕ_1 (Fig. 6.13),

phase2 – corresponds to the waveform ϕ_2,

static – permanently closed switch,

sign "–" denotes connection.

First cell (upper)

Connections:
EI – [S-1(closed)] – [II-1(UL)] – [S1-1(static)] – [OA-1(negative opamp input)] –
– [SW-6(static)] – IO – EO.

Second cell (lower)

Connections:
EI – [S-1(closed)] – [II-1(UL)] – [S1-1(phase2)] – [C1-1(5)] – [SW1-1(phase2)] –
– [OA(negative opamp input)] – [C-2(250)] – [SW5-1(static)] – IO – EO.
[S8(close)] – [OA(positive opamp input)].
[II-2(U)] – [S2-1(static)] – [OA-2(negative opamp input)].

Complementary switches:
[S1-2(phase1)].
[SW1-2(phase1)].

6.4. Appendix IV – Nanostructures Data

6.4.1. EGF Protein in PDB Format

The Protein Data Bank (PDB) file determines three-dimensional structures of molecules described in a standard format. The PDB files contain atomic coordinates in the macromolecules in angstroms, structure information, bibliographic data, crystallographic structure parameters, and NMR experimental data.

The PDB file may be viewed as a collection of record types. Each record type contains of one or more lines (each line consists of 80 columns). Further, each record is divided into fields. A text file generally contains several different types of records, which are arranged in a particular order to describe a structure of molecule. The keywords such as ATOM, HETATM, END, etc. in the beginning of the record, determine the type of record and the meaning of the fields after the keyword.

The format of data for records ATOM and HETATM has the following form:

```
FORMAT(6A1,I5,1X,A4,A1,A3,1X,A1,I4,A1,3X,3F8.3,2F6.2,1X,I3,2X,A4,2A2)
```

Column	Content
1-6	"ATOM" or "HETATM"
7-17	Atom description
18-27	Residue description
31-54	Orthogonal coordinates in angstroms
55-80	Additional data (modified in 1992 and 1996)

Residues occur in order starting from the N-terminal residue for proteins and 5' - terminus for nucleic acids.

ATOM records present the atomic coordinates for standard residues and atom characterization in a molecule. In the field "serial" (columns 7-11 in the atom description), the atom serial number in molecule is present. The atom name is in the field "name (columns 13-16). The first one or two characters of the atom name consists of the chemical symbol for the atom type. All the atom names beginning with "C" are carbon atoms, "N" indicates a nitrogen, "O" indicates oxygen, "P" phosphorus, and so forth. The next character is the remoteness indicator code, which have to be transliterated in the following manner:

$\alpha - A, \beta - B, \gamma - G, \delta - D, \varepsilon - E, \zeta - Z, \eta - H.$

In the field "resName" (column 17) of ATOM record, is an atom branch indicator, if required.

HETATM records present the atomic coordinates for atoms within "non-standard" groups (only the twenty common amino acids and five nucleic acids plus inosine are treated as "standard").

TER records are interpreted as breaks in the main molecule's backbone.

The END record marks the end of the PDB file.

The short PDB format description provided here will suffice for general inspection of the file, the complete PDB file specification can be found in thePDB documentation [CCDE96].

The EGF (Epidermal Growth Factor) protein consisting of 53 amino acids (asparagine at the N-terminus and arginine at C-terminus) in PDB format has the following form:

```
HEADER    Epidermal Growth Factor (EGF) straight chain
COMPND
SOURCE
ATOM      1  N   ASN     1       0.000   0.000   0.000
ATOM      2  CA  ASN     1       0.000   0.000   1.500
ATOM      3  C   ASN     1       1.413   0.000   2.034
ATOM      4  O   ASN     1       2.283  -0.728   1.585
ATOM      5  CB  ASN     1      -0.698  -1.273   2.014
ATOM      6  CG  ASN     1      -0.676  -1.234   3.523
ATOM      7  OD1 ASN     1      -1.161  -2.119   4.209
ATOM      8  ND2 ASN     1      -0.270  -0.051   4.004
ATOM      9 1H   ASN     1      -0.680   0.680  -0.340
ATOM     10 2H   ASN     1      -0.277  -0.921  -0.340
ATOM     11 3H   ASN     1       0.921   0.277  -0.340
ATOM     12  HA  ASN     1      -0.505   0.917   1.871
ATOM     13 1HB  ASN     1      -0.123  -2.165   1.688
ATOM     14 2HB  ASN     1      -1.758  -1.270   1.688
ATOM     15 1HD2 ASN     1      -0.020   0.690   3.349
ATOM     16 2HD2 ASN     1       0.019   0.013   4.980
ATOM     17  N   SER     2       1.587   0.874   3.034
ATOM     18  CA  SER     2       2.886   1.023   3.684
ATOM     19  C   SER     2       2.753   1.073   5.188
ATOM     20  O   SER     2       1.906   1.747   5.749
ATOM     21  CB  SER     2       3.542   2.339   3.228
ATOM     22  OG  SER     2       4.789   2.440   3.877
ATOM     23  H   SER     2       0.786   1.432   3.528
ATOM     24  HA  SER     2       3.531   0.157   3.427
ATOM     25 1HB  SER     2       2.930   3.197   3.575
ATOM     26 2HB  SER     2       3.754   2.286   2.139
ATOM     27  HG  SER     2       5.182   3.245   3.592
.
.
```

49 successive amino acids.

```
ATOM    757  N   LEU    52      92.832   7.384 147.849
ATOM    758  CA  LEU    52      92.855   7.541 149.300
ATOM    759  C   LEU    52      94.247   7.354 149.857
ATOM    760  O   LEU    52      94.976   6.442 149.506
ATOM    761  CB  LEU    52      91.944   6.481 149.947
ATOM    762  CG  LEU    52      91.969   6.647 151.478
ATOM    763  CD1 LEU    52      91.058   5.587 152.125
ATOM    764  CD2 LEU    52      93.410   6.464 151.991
ATOM    765  H   LEU    52      93.324   6.614 147.396
ATOM    766  HA  LEU    52      92.515   8.563 149.568
ATOM    767 1HB  LEU    52      92.309   5.468 149.680
ATOM    768 2HB  LEU    52      90.905   6.614 149.579
ATOM    769  HG  LEU    52      91.604   7.660 151.745
ATOM    770 1HD1 LEU    52      91.077   5.708 153.228
ATOM    771 2HD1 LEU    52      91.424   4.574 151.858
ATOM    772 3HD1 LEU    52      90.019   5.721 151.757
ATOM    773 1HD2 LEU    52      93.426   6.584 153.094
ATOM    774 2HD2 LEU    52      94.066   7.230 151.527
ATOM    775 3HD2 LEU    52      93.770   5.449 151.725
ATOM    776  N   ARG    53      94.572   8.290 150.759
ATOM    777  CA  ARG    53      95.878   8.282 151.413
ATOM    778  C   ARG    53      95.757   8.519 152.899
ATOM    779  O   ARG    53      94.993   9.438 153.267
ATOM    780  CB  ARG    53      96.753   9.405 150.827
ATOM    781  CG  ARG    53      98.130   9.396 151.516
ATOM    782  CD  ARG    53      99.006  10.520 150.930
ATOM    783  NE  ARG    53     100.302  10.512 151.579
ATOM    784  CZ  ARG    53     101.240  11.415 151.224
ATOM    785  NH1 ARG    53     102.447  11.408 151.829
ATOM    786  NH2 ARG    53     100.972  12.326 150.264
ATOM    787  OXT ARG    53      96.429   7.778 153.649
ATOM    788  H   ARG    53      93.881   9.007 150.976
ATOM    789  HA  ARG    53      96.361   7.294 151.263
ATOM    790 1HB  ARG    53      96.260  10.384 150.999
ATOM    791 2HB  ARG    53      96.885   9.239 149.737
ATOM    792 1HG  ARG    53      98.623   8.417 151.344
ATOM    793 2HG  ARG    53      97.998   9.563 152.606
ATOM    794 1HD  ARG    53      98.513  11.499 151.103
ATOM    795 2HD  ARG    53      99.138  10.354 149.841
ATOM    796  HE  ARG    53     100.505   9.824 152.305
ATOM    797 1HH1 ARG    53     103.156  12.090 151.560
ATOM    798 2HH1 ARG    53     102.650  10.719 152.554
ATOM    799 1HH2 ARG    53     101.681  13.008 149.996
ATOM    800 2HH2 ARG    53     100.060  12.331 149.808
END
```

6.4.2. Graphic Presentation of Molecules

Figs. 6.14 and 6.15 present different graphic representations [Sayl01] of the DNA molecule (file 208d.pdb) and molecules of selected amino acids: L-arginine and L-proline from Protein Data Bank.

6.4.3. Supercomputing in Nanostructures Computations

Completion of the system of massive computations for simulation of conformation polypeptide chain processes, switching phenomena, and dynamics of the translation, in case of short amino acids chain needs very fast PC computer. In case of small or medium size protein especially when optimization procedures are performed, the use of supercomputer system is necessary (p. 6.2.1). In case when a very long data chain have to be process in connection

with simulation of structure behavior described with Hardware Description Language, the bi-directional communucation between disk files and contents of the procedures body of HDL during simulation is fulfilled [Znam01b, ZnZu02b, Znam00, ZnPa01, Grzy00].

a) b)

Fig. 6.14. Representations of molecule. User-set angles. Zoom equals to 150. Molecule DNA: a) ribbons representation, b) spacefill representation

Rys. 6.14. Wizualizacja molekuł. Kąty obserwacji ustawione przez użytkownika. Zoom 150. Molekuła DNA: a) reprezentacja wstęgowa, b) reprezentacja kulowa

a) b)

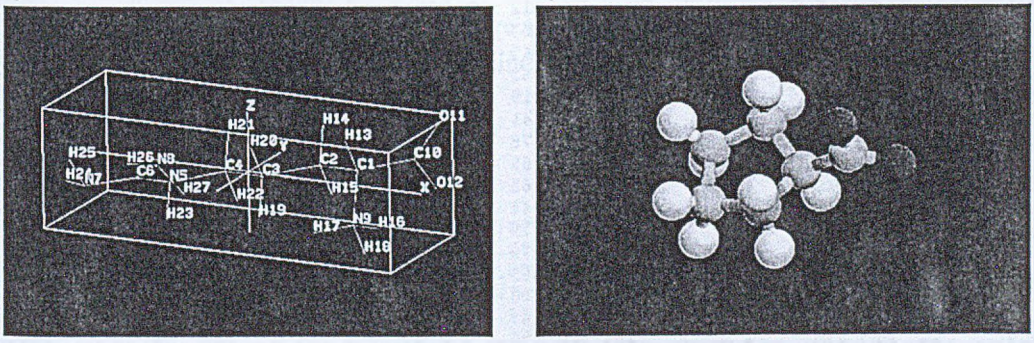


Fig. 6.15. Representations of molecule: a) L-arginine amino acid – wireframe representation (active options: atoms' description, boundbox of molecule, and view of *x,y,z* axes), b) L-proline - ball & sticks representation

Rys. 6.15. Wizualizacja molekuł: a) aminokwas L-arginina - reprezentacja sitowa (aktywne opcje widoku: opis atomów, obrys molekuły oraz osie współrzędnych *x, y, z*), b) L-prolina – reprezentacja kulowo-belkowa

6.4.4. Polypeptide A in PDB Format

The polypeptide A (SEQ1) containing seven amino acids (Fig. 4.15):
Methionine – Alanine – Glycine – Histidine – Glycine – Alanine – Histidine

in the PDB format has the following form:

```
HEADER    SEQ1 (Polypeptide A)
COMPND
SOURCE
ATOM      1  N   MET     1       0.000   0.000   0.000
ATOM      2  CA  MET     1       0.000   0.000   1.500
ATOM      3  C   MET     1       1.413   0.000   2.034
ATOM      4  O   MET     1       2.283  -0.728   1.585
ATOM      5  CB  MET     1      -0.698  -1.273   2.014
ATOM      6  CG  MET     1      -0.698  -1.273   3.554
ATOM      7  SD  MET     1      -1.524  -2.782   4.147
ATOM      8  CE  MET     1      -1.332  -2.431   5.922
ATOM      9 1H  MET     1       0.376   0.885  -0.340
ATOM     10 2H  MET     1      -0.957  -0.088  -0.340
ATOM     11 3H  MET     1       0.602  -0.750  -0.340
ATOM     12  HA  MET     1      -0.505   0.917   1.871
ATOM     13 1HB  MET     1      -0.152  -2.167   1.645
ATOM     14 2HB  MET     1      -1.744  -1.294   1.645
ATOM     15 1HG  MET     1      -1.197  -0.353   3.923
ATOM     16 2HG  MET     1       0.347  -1.199   3.923
ATOM     17 1HE  MET     1      -1.771  -3.232   6.554
ATOM     18 2HE  MET     1      -1.777  -1.454   6.203
ATOM     19 3HE  MET     1      -0.269  -2.280   6.203
ATOM     20  N   ALA     2       1.587   0.874   3.034
ATOM     21  CA  ALA     2       2.886   1.023   3.684
ATOM     22  C   ALA     2       3.289  -0.235   4.415
ATOM     23  O   ALA     2       2.511  -0.867   5.111
ATOM     24  CB  ALA     2       2.817   2.165   4.715
ATOM     25  H   ALA     2       0.786   1.432   3.328
ATOM     26  HA  ALA     2       3.661   1.236   2.919
ATOM     27 1HB  ALA     2       3.805   2.277   5.208
ATOM     28 2HB  ALA     2       2.048   1.926   5.480
ATOM     29 3HB  ALA     2       2.553   3.112   4.200
ATOM     30  N   GLY     3       4.573  -0.563   4.211
ATOM     31  CA  GLY     3       5.154  -1.749   4.833
ATOM     32  C   GLY     3       5.023  -2.963   3.945
ATOM     33  O   GLY     3       4.491  -2.918   2.848
ATOM     34  H   GLY     3       5.131   0.041   3.608
ATOM     35 1HA  GLY     3       6.234  -1.578   5.020
ATOM     36 2HA  GLY     3       4.625  -1.965   5.785
ATOM     37  N   HIS     4       5.550  -4.065   4.495
ATOM     38  CA  HIS     4       5.523  -5.344   3.791
ATOM     39  C   HIS     4       4.116  -5.879   3.664
ATOM     40  O   HIS     4       3.328  -5.879   4.596
ATOM     41  CB  HIS     4       6.395  -6.365   4.544
ATOM     42  CG  HIS     4       6.367  -7.678   3.821
ATOM     43  ND1 HIS     4       7.219  -8.067   2.848
ATOM     44  CD2 HIS     4       5.485  -8.679   4.027
ATOM     45  CE1 HIS     4       6.864  -9.309   2.454
ATOM     46  NE2 HIS     4       5.792  -9.687   3.183
ATOM     47  H   HIS     4       5.971  -3.985   5.421
ATOM     48  HA  HIS     4       5.930  -5.212   2.767
ATOM     49 1HB  HIS     4       5.999  -6.502   5.572
ATOM     50 2HB  HIS     4       7.440  -5.993   4.592
ATOM     51  HD1 HIS     4       7.995  -7.519   2.477
ATOM     52  HD2 HIS     4       4.661  -8.675   4.756
ATOM     53  HE1 HIS     4       7.360  -9.907   1.676
ATOM     54  HE2 HIS     4       5.301 -10.578   3.108
ATOM     55  N   GLY     5       3.847  -6.342   2.436
ATOM     56  CA  GLY     5       2.538  -6.902   2.113
ATOM     57  C   GLY     5       1.575  -5.833   1.655
ATOM     58  O   GLY     5       1.889  -4.657   1.577
ATOM     59  H   GLY     5       4.585  -6.292   1.733
ATOM     60 1HA  GLY     5       2.643  -7.641   1.292
ATOM     61 2HA  GLY     5       2.108  -7.384   3.016
ATOM     62  N   ALA     6       0.365  -6.323   1.353
```

```
ATOM     63  CA  ALA     6      -0.707  -5.447   0.889
ATOM     64  C   ALA     6      -2.067  -5.984   1.267
ATOM     65  O   ALA     6      -2.316  -7.178   1.294
ATOM     66  CB  ALA     6      -0.655  -5.337  -0.646
ATOM     67  H   ALA     6       0.215  -7.327   1.456
ATOM     68  HA  ALA     6      -0.595  -4.445   1.355
ATOM     69 1HB  ALA     6      -1.470  -4.671  -0.996
ATOM     70 2HB  ALA     6      -0.785  -6.345  -1.092
ATOM     71 3HB  ALA     6       0.325  -4.914  -0.952
ATOM     72  N   HIS     7      -2.943  -5.013   1.562
ATOM     73  CA  HIS     7      -4.314  -5.331   1.952
ATOM     74  C   HIS     7      -5.280  -5.115   0.812
ATOM     75  O   HIS     7      -5.204  -4.027   0.201
ATOM     76  CB  HIS     7      -4.725  -4.451   3.147
ATOM     77  CG  HIS     7      -6.133  -4.777   3.548
ATOM     78  ND1 HIS     7      -6.506  -5.711   4.448
ATOM     79  CD2 HIS     7      -7.250  -4.187   3.071
ATOM     80  CE1 HIS     7      -7.853  -5.698   4.528
ATOM     81  NE2 HIS     7      -8.313  -4.757   3.677
ATOM     82  OXT HIS     7      -6.082  -6.042   0.565
ATOM     83  H   HIS     7      -2.623  -4.047   1.506
ATOM     84  HA  HIS     7      -4.375  -6.397   2.255
ATOM     85 1HB  HIS     7      -4.662  -3.381   2.857
ATOM     86 2HB  HIS     7      -4.043  -4.647   4.001
ATOM     87  HD1 HIS     7      -5.880  -6.319   4.976
ATOM     88  HD2 HIS     7      -7.287  -3.384   2.321
ATOM     89  HE1 HIS     7      -8.469  -6.343   5.173
ATOM     90  HE2 HIS     7      -9.292  -4.518   3.519
END
```

6.4.5. Polypeptide B in PDB Format

The polypeptide B (SEQ2) containing five amino acids (Fig. 4. 17):

Methionine – Alanine – Glycine – Histidine – Glycine

in the PDB format has the following form:

```
HEADER    SEQ2 (Polypeptide B)
COMPND
SOURCE
ATOM      1  N   MET     1       0.000   0.000   0.000
ATOM      2  CA  MET     1       0.000   0.000   1.500
ATOM      3  C   MET     1       1.413   0.000   2.034
ATOM      4  O   MET     1       2.278  -0.740   1.597
ATOM      5  CB  MET     1      -0.698  -1.273   2.014
ATOM      6  CG  MET     1      -0.698  -1.273   3.554
ATOM      7  SD  MET     1      -1.524  -2.782   4.147
ATOM      8  CE  MET     1      -1.332  -2.431   5.922
ATOM      9 1H  MET     1       0.391   0.878  -0.340
ATOM     10 2H  MET     1      -0.959  -0.071  -0.340
ATOM     11 3H  MET     1       0.589  -0.760  -0.340
ATOM     12  HA  MET     1      -0.505   0.917   1.871
ATOM     13 1HB  MET     1      -0.152  -2.167   1.645
ATOM     14 2HB  MET     1      -1.744  -1.294   1.645
ATOM     15 1HG  MET     1      -1.197  -0.353   3.923
ATOM     16 2HG  MET     1       0.347  -1.199   3.923
ATOM     17 1HE  MET     1      -1.771  -3.232   6.554
ATOM     18 2HE  MET     1      -1.777  -1.454   6.203
ATOM     19 3HE  MET     1      -0.269  -2.280   6.203
ATOM     20  N   ALA     2       1.593   0.889   3.020
ATOM     21  CA  ALA     2       2.892   1.041   3.667
ATOM     22  C   ALA     2       2.912   0.394   5.032
ATOM     23  O   ALA     2       2.051   0.604   5.870
ATOM     24  CB  ALA     2       3.204   2.538   3.852
```

```
ATOM     25  H   ALA     2       0.795   1.457   3.304
ATOM     26  HA  ALA     2       3.674   0.554   3.048
ATOM     27 1HB  ALA     2       4.192   2.651   4.344
ATOM     28 2HB  ALA     2       2.420   3.002   4.486
ATOM     29 3HB  ALA     2       3.227   3.034   2.859
ATOM     30  N   GLY     3       3.965  -0.417   5.204
ATOM     31  CA  GLY     3       4.163  -1.137   6.459
ATOM     32  C   GLY     3       4.469  -0.194   7.598
ATOM     33  O   GLY     3       3.912  -0.271   8.681
ATOM     34  H   GLY     3       4.624  -0.517   4.432
ATOM     35 1HA  GLY     3       3.237  -1.693   6.716
ATOM     36 2HA  GLY     3       5.019  -1.835   6.355
ATOM     37  N   HIS     4       5.402   0.714   7.281
ATOM     38  CA  HIS     4       5.836   1.716   8.250
ATOM     39  C   HIS     4       5.206   3.061   7.979
ATOM     40  O   HIS     4       5.201   3.572   6.872
ATOM     41  CB  HIS     4       7.370   1.848   8.202
ATOM     42  CG  HIS     4       7.816   2.877   9.197
ATOM     43  ND1 HIS     4       8.142   2.645  10.486
ATOM     44  CD2 HIS     4       7.961   4.199   8.962
ATOM     45  CE1 HIS     4       8.489   3.823  11.048
ATOM     46  NE2 HIS     4       8.377   4.783  10.105
ATOM     47  H   HIS     4       5.800   0.684   6.342
ATOM     48  HA  HIS     4       5.537   1.399   9.271
ATOM     49 1HB  HIS     4       7.681   2.161   7.183
ATOM     50 2HB  HIS     4       7.832   0.870   8.450
ATOM     51  HD1 HIS     4       8.129   1.739  10.954
ATOM     52  HD2 HIS     4       7.772   4.709   8.006
ATOM     53  HE1 HIS     4       8.808   3.974  12.090
ATOM     54  HE2 HIS     4       8.573   5.776  10.235
ATOM     55  N   GLY     5       4.666   3.610   9.077
ATOM     56  CA  GLY     5       4.008   4.912   9.020
ATOM     57  C   GLY     5       4.983   6.013   8.677
ATOM     58  O   GLY     5       4.642   6.813   7.779
ATOM     59  OXT GLY     5       6.056   6.041   9.317
ATOM     60  H   GLY     5       4.729   3.091   9.952
ATOM     61 1HA  GLY     5       3.222   4.896   8.237
ATOM     62 2HA  GLY     5       3.564   5.146  10.010
END
```

6.4.6. Nascent Protein Folding Simulation Algorithm

The basic assumption for the construction of two-phase NPF Simulation Algorithm is an observation, that the new amino-acid appearing from the ribosome rotates the existing chain of amino acids in a such manner, that the torsion angles on the new peptide bond, accordingly with minimization of potential energy of the structure {*new amino acid*}/{*existing amino acid chain*} are determined, and next, the conformation of the whole structure is somewhat modified to minimize the potential energy of {*new existing amino acid chain*}. The first minimization plays a crucial role because of dimensions of peptide chain in comparison with the new molecule attached.

Initialization

The space defining available regions of φ and ψ angles (Fig. 4.14) is quantized and translated to the linear vector of available coordinates. The two first amino acids adopt the conformation minimizing expression

$$\min_{\varphi_0,\psi_0,\varphi_1,\psi_1} E_2(\varphi_0,\psi_0,\varphi_1,\psi_1), \tag{6.2}$$

where E_2 is a potential energy of the system of two amino acids, φ_0 and ψ_0 are the torsion angles of the first amino acid, as well as φ_1 and ψ_1 are the torsion angles of the second amino acid (Fig. 6.16).

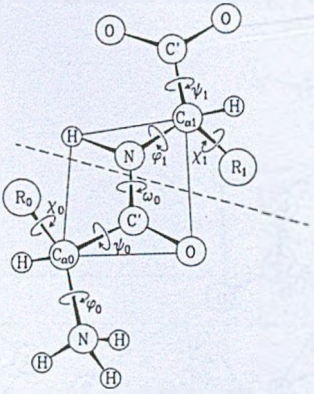


Fig. 6.16. Initialization of simulation
Rys. 6.16. Faza inicjalizacji symulacji

First Phase of Simulation

When the third residue appears (#2 in Fig.6.17a), the following expression is minimized

$$\min_{\varphi_2,\psi_2} E_3(\varphi_2,\psi_2,\varphi_{0f},\psi_{0f},\varphi_{1f},\psi_{1f}), \tag{6.3}$$

where E_3 is a potential energy of the system of three amino acids, $\varphi_{0f},\psi_{0f},\varphi_{1f},\psi_{1f}$ are the torsion angles determined in the initialization.

The first phase for fourth amino acid is preceded by the second phase which tunes the existing, whole chain to get the minimal potential energy.

Accordingly, for the fourth amino acid we minimize the expression

$$\min_{\varphi_3,\psi_3} E_4(\varphi_3,\psi_3,\varphi_{2s},\psi_{2s},\varphi_{0fs},\psi_{0fs},\varphi_{1fs},\psi_{1fs}), \tag{6.4}$$

where E_4 is a potential energy of the system of four amino acids, φ_{2s}, ψ_{2s}, φ_{0fs}, ψ_{0fs}, φ_{1fs}, ψ_{1fs} are the torsion angles (Fig. 6.17b) determined in the second phase for the three amino acids.

Second Phase of Simulation

For the consecutive residues, bonded to the growing chain, the global tuning after the first phase takes place.

Along the backbone of the chain (Fig. 6.18), the torsion angles are changed in the four directions: $+k\Delta\varphi_i$, $-k\Delta\varphi_i$, $+k\Delta\psi_i$, and $-k\Delta\psi_i$, including the current φ_i and ψ_i ($i = 0, 1, \ldots, n$) angles. Values of $\Delta\varphi_i$ and $\Delta\psi_i$ determine the amplitudes of reversible changes of torsion angles along the chain, and k is a positive and decreasing parameter during the consecutive steps of the minimization of potential energy of the chain.

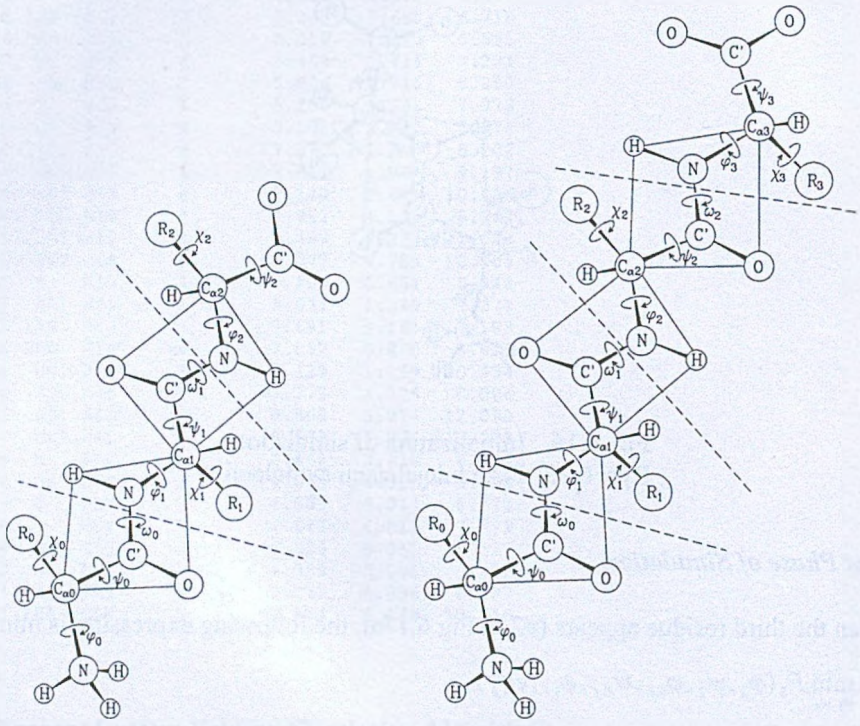


Fig. 6.17. First phase of simulation: a) the three residues, b) the four residues
Rys. 6.17. Pierwsza faza symulacji: a) trzy aminokwasy, b) cztery aminokwasy

The parameter k can be constant in one iteration step, as well as may be a function of selected parameters.

6.4.7. Software Supporting the Simulation of Conformation Switching Processes in the Nanostructures

The documentation, codes of programs, their modified and extended versions including the Nascent Protein Folding Simulation, Dynamic Programming (the subroutines library) and Monte Carlo algorithms implementation, programs for nanostructures spatial shape manipulation, force field files, potential energy programs, quantized Ramachandran restriction data files, format translators, visualization programs, modified quantized Ramachandran restriction

data files, nanostructures library from the Internet accessible databases, and software specialized tools are gathered in the two internal reports:

L. Znamirowski: "Polypeptides – Synthesis and Visualization", (Internal Report No. 3/ September 2001), Institute of Informatics, Silesian University of Technology, Gliwice 2001,

L. Znamirowski: "Conformational Switching in the Nanoprocesses", (Internal Report No. 2/ 04), Institute of Informatics, Silesian University of Technology, Gliwice 2004.

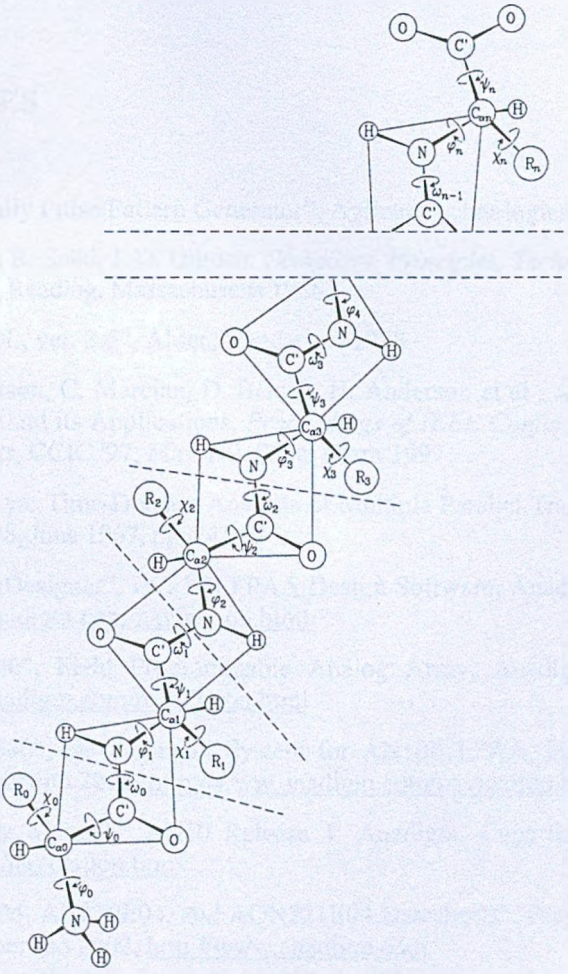


Fig. 6.18. Chain of *n* amino acids – the second phase of simulation
Rys. 6.18. Łańcuch *n* aminokwasów – druga faza symulacji

6.4.8. Signal Transduction Cascades Data

The basic, in descriptive form results from biochemical research in the area of signal pathways in biological nanostructures representing the signal transduction cascades from [Berr85,

BioC03, Cell03, Roco02, NoZa04, FuSh98, LBZM01, BrCa00, Ray99, Stry94] are partly gathered in:

L. Znamirowski: "Signal Cascades", (Internal Report No. 3), Institute of Informatics, Silesian University of Technology, Gliwice 2003.

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SWITCHING

VLSI Structures
Reprogrammable FPAA Structures
Nanostructures

ABSTRACT

The work concerns the problem of switching processes in VLSI technology, reprogrammable analog arrays technology, and nanotechnology.

Informatics is a discipline of science exploring the laws of processes of coding, processing, storing and transferring information or data. The movement and processing of information is indissolubly connected with the switching of states of structures carrying the data. In general, the changes of structure state can be forced through the changes of carried data parameters with unchanged structure configuration, through the switching of structure configuration or switching of the structure conformation. Switching is exhibited in different technologies by different basic elements (basic structures or building blocks) and specified operations performed on them in order to obtain the object or product with desirable properties including also the dynamic changes of those properties. Dealing in turn with so different cases as VLSI structures, FPAA (Field Programmable Analog Array) structures and nanostructures, it is possible to notice, that the common feature takes a stand in solving the tasks related with them, rely on choice of certain basic elements critical for structure behavior as e.g. multiconductor transmission lines (MTL), configurations of FPAA substructures or whole FPAA systems, molecule conformations, and it is operated on them analyzing the internal switching processes.

The design of interconnects in a high-speed integrated circuits and systems requires analysis and computer simulation based on interconnects models in the form of coupled, multiconductor transmission lines. The fundamental parameters for matrix description (or modeling, simulation and design) of MTL include the capacitance matrices. Precisely, these are the matrices per-unit of length, the capacitance coefficients matrix called Maxwell matrix of MTL and the two-terminal capacitance matrix. If the two-terminal matrix is known, the Maxwell matrix used for MTL switching characteristics estimation, can be computed from the two-terminal matrix.

In the work, two methods of determination of the Maxwell matrix from measurements are presented: passive, indirect measurements and measurements with active separation.

The measurements were performed basing on fabricated VLSI test structures named ST2 and AF4. The measurement results are complemented with the accuracy analysis.

Scaling of structures is conformed to fast switching, high-speed integrated VLSI/ULSI integrated circuits design. In case when the geometrical dimensions decrease, multiconductor interconnections between parts of a system become strongly coupled MTL, which in switching moments have to be recharged with small geometry devices. In the work the method and numerical computations of scaled (in geometrical sense) MTL for its energetical characterization is presented. This can be used for proper design of MTL geometrical parameters in a VLSI/ULSI structures working with a high-speed switching. The results of measurements of the switching delay in the scaled in dimensions VLSI gates, are also included.

Poor matching of the switched MTL reveals with reflections extending the time of switching and can be source of switching noises. The method of so called diagonal matching is presented in the work.

The time of switching in the high-speed planar VLSI structures (driver and receiver gates connected via the long microstrip line) depends on dielectric properties of substrate under the signal and ground microstrip lines. Most important for fast switching is recharging of dielectric in the presence of the dielectric absorption phenomenon. In the work, the model of dielectric absorption and its identification algorithm based on the experimental data is presented. This model can be used for simulation of switching transients in the interconnections of different length for given technology, taking into account the dielectric absorption.

Nowadays, it is apparent that many designs are evolving towards mixed-signal systems. In these kind of circuits in CMOS technology, the analog part of a system and an interface are composed frequently basing on switched capacitor (SC) technology and in the newest solution basing on field programmable analog arrays. There are two main weak points in fast switching of reconfigurable FPAA: firstly, the time of download of the configuration from supporting program or EEPROM memory with the time of transients in a FPAA chip when the download is finished and the chip undertakes its function, and secondly, for recently accessible FPAAs, there is no possibility of switching its parameters values and a part of active structure on-the-fly (during FPAA operation).

In the work, the solution of fast switching of the part of working FPAA for adaptive operation is presented. The solution is based on external control of one or few CAB (Configurable Analog Block) in the working FPAA. The solution of the download time problem in FPAA chip operating in continuous time fashion is based on parallelization of the FPAAs and "hiding" of the download time and time of transients after download. Finally, the applications of the modified, fast switched FPAAs systems for adaptive and predictive control with possible application in the microreactors control have been presented.

In the nanonetworks, an information is transferred through the state of moving molecules. In a short-distance communication (inside the closed area determined by the borders of nanoprocess) the state of the signaling molecules is forced through the binding via hydrogen or co-

valent bonds of another molecule or through the interaction of the environment's parameters. These processes in biological nanonetworks are performed in the signal transduction cascades and the same procedures are applied in the nanotechnical systems of informatics. We considered these processes with emphasis on the fusion of cascades.

In general, these interactions lead to the switching of conformations of the molecule. In the work, we focused on biocompatible nanostructures introducing the standard, formal description of molecular structures, methodology of modeling and simulation of the conformational changes, and hierarchical description of nanonetworks useful in the switching conformation studies. The simulation methodologies based on the dynamic programming, Monte Carlo and Nascent Protein Folding algorithms are investigated. Moreover, nanotechnological, two-stage production processes based on the "gluey matrix" concept are discussed.

PRZEŁĄCZANIE

Struktury VLSI
Reprogramowalne struktury FPAA
Nanostruktury

STRESZCZENIE

W pracy rozważono zagadnienie procesów przełączania w strukturach implementowanych w technologiach monolitycznych układów VLSI, reprogramowalnych macierzy analogowych FPAA (Field Programmable Analog Array) oraz nanotechnologii.

Informatyka jest dyscypliną nauki badającą prawa rządzące procesami kodowania, przetwarzania, przechowywania i przesyłania informacji lub danych. W fizycznej implementacji tych procesów należy rozważać rodzaj technologii wykorzystanej do budowy elementów i obiektów reprezentujących pracujący system informatyki. Ruch i przetwarzanie informacji (włączając pamiętanie danych) są nierozerwalnie związane z przełączaniem stanów struktur przenoszących dane. Ogólnie, zmiany stanu struktury przenoszącej dane mogą być wymuszane zmianami parametrów sygnałów reprezentujących dane przy niezmienionej konfiguracji struktury, poprzez przełączanie konfiguracji struktury lub przełączanie konformacji struktury.

W pracy rozważono wybrane zagadnienia procesów przełączania w strukturach implementowanych w wymienionych technologiach determinujące dynamikę, poprawność i ograniczenia w realizacji tych procesów, umożliwiających budowę pożądanych obiektów lub struktur na bazie wybranego zbioru elementów podstawowych dla danej technologii, krytycznego dla właściwości i zachowania tworzonych obiektów lub struktur.

Problematyka pracy została tak sformułowana, aby uzyskane rezultaty eksperymentalne i wyniki symulacji mogły być wykorzystane w analizie i projektowaniu przełączanych struktur z wykorzystaniem odpowiedniego oprogramowania CAD/CAE.

Projektowanie połączeń w układach scalonych i systemach z dużą szybkością przełączania wymaga analizy i symulacji komputerowej bazującej na modelach sprzężonych wielolinii transmisyjnych (MTL). Podstawowym parametrem w opisie macierzowym wielolinii MTL (dla modelowania, symulacji i projektowania) są macierze pojemności. Dokładnie, macierze pojemności na jednostkę długości, do których zalicza się macierz współczynników pojemności nazywaną macierzą Maxwella oraz macierz, której elementami są pojemności dwukońcówkowe. Jeśli jest znana macierz pojemności dwukońcówkowych, to na jej podstawie

można obliczyć macierz Maxwella wykorzystywaną w estymacji charakterystyk przełączania wielolinii MTL.

W pracy przedstawiono dwie metody wyznaczania macierzy Maxwella na podstawie pomiarów: metodę pomiaru pośredniego oraz metodę pomiaru z aktywną separacją sieci pojemności. Pomiary zostały wykonane dla dwu zaprojektowanych i wykonanych struktur testowych VLSI nazwanych ST2 i AF4. Dla obu metod przeprowadzono analizę błędu pomiaru pozwalającą wybrać metodę dla danego zastosowania.

Skalowanie struktur jest stosowane w projektowaniu szybko przełączających układów VLSI/ULSI. W przypadku zmniejszania wymiarów geometrycznych wielolinia staje się strukturą o silnych sprzężeniach pojemnościowych i musi być szybko przeładowywana przez przyrządy półprzewodnikowe małej geometrii. W pracy przedstawiono metodę oraz obliczenia numeryczne pozwalające scharakteryzować przeskalowaną wielolinię MTL w sensie energetycznym, co może być wykorzystane w projektowaniu geometrii wielolinii w szybko przełączających strukturach VLSI/ULSI. Zaprezentowano także wyniki pomiarów czasu opóźnienia przełączania w skalowanych bramkach VLSI.

Niewłaściwe dopasowanie obciążenia wielolinii MTL prowadzi do odbić wydłużających czas przełączania. W pracy przedstawiono metodę dopasowania niwelującą te efekty, nazwaną metodą dopasowania diagonalnego.

W strukturach VLSI istotny wpływ na szybkość przełączania bramek sterowanych z odległych źródeł poprzez mikrolinie transmisyjne ma podłoże struktury monolitycznej. W pracy przeanalizowano zależność czasu przełączania od właściwości dielektrycznych podłoża pod liniami sygnałowymi i ziemi. Degradujące szybkość przełączania jest tu zjawisko absorpcji dielektrycznej. W pracy przedstawiono model tego zjawiska i opracowano algorytm identyfikacji parametrów modelu dla danych uzyskanych z pomiarów struktury testowej ST2. Model ten wykorzystano w symulacji stanów nieustalonych przełączania w linii o zmienianej długości łączącej inwertery nadajnika i odbiornika VLSI z uwzględnieniem zjawiska absorpcji dielektryka.

Układy cyfrowe VLSI wykorzystuje się w implementacji algorytmów obliczeniowych o wysokim stopniu złożoności i dużej dokładności obliczeń zwykle przy niższych częstotliwościach sygnałów przetwarzanych, gdy rozpraszanie mocy w trakcie obliczeń nie jest krytyczne. Układy analogowe wykazują przewagę w aplikacjach przy wyższych częstotliwościach sygnałów przetwarzanych oraz wtedy, gdy istotna jest mała moc rozpraszania w trakcie przetwarzania. Jednakże dokładność układów analogowych jest ograniczona i nie mogą z natury rzeczy realizować algorytmów o dużej złożoności. We współcześnie realizowanych algorytmach o dużej złożoności i wymaganiach co do szybkości przetwarzania i ograniczenia mocy rozpraszania przez system, podział na układy realizujące tylko funkcje analogowe lub tylko cyfrowe staje się nieuzasadniony. Z drugiej strony rosną wymagania związane z elastycznością hardware'u, który w trakcie pracy powinien być dynamicznie rekonfigurowalny. Problem ten rozwiązują w zakresie układów cyfrowych układy FPGA, natomiast typowa

technologia VLSI układów analogowych nie pozwala na w pełni elastyczne zmiany konfiguracji pracującego układu. Nowe architektury oraz technologie budowy układów analogowych, bazujące na zasadzie przełączanych pojemności lub prądów, rozwiązały problem rekonfiguracji układów analogowych przez wprowadzenie technologii FPAA pozwalającej przez wpis konfiguracji rekonfigurować całą strukturę. W pracy rozwinięto tę koncepcję dalej, wprowadzając rozwiązania architektury pracującego systemu zbudowanego na bazie układów FPAA (w technologii SC), zapewniające dynamiczną rekonfigurację części struktury w trakcie nieprzerwanej pracy układu FPAA lub systemu zbudowanego na kilku FPAA. W chwili obecnej, z punktu widzenia szybkiej rekonfiguracji układów FPAA, występują dwa słabe punkty: po pierwsze, długi czas wpisu konfiguracji i stany nieustalone poprzedzające rozpoczęcie realizacji zaprogramowanej funkcji po zakończeniu procesu jej wpisu i po drugie, brak możliwości częściowego przełączania wartości parametrów i przełączania funkcji części struktury pracującej w sposób ciągły („w biegu"). W pracy przedstawiono rozwiązanie radykalnie przyśpieszające przełączanie wewnętrznych struktur pracującej struktury FPAA poprzez zewnętrzne sterowanie jednego lub kilku wewnętrznych układów CAB (Configurable Analog Block) realizujących odpowiednie makra. Problem eliminacji czasu wpisu konfiguracji (przerywającego ciągłą pracę układu) przy zapewnieniu ciągłej pracy został rozwiązany przez zrównoleglenie współpracujących FPAA i „ukrycie" czasu wpisu konfiguracji oraz stanów nieustalonych po wpisie. Tak zmodyfikowane układy FPAA wykorzystane zostały w eksperymentach realizujących podstawowe funkcje sterowania adaptacyjnego i predykcyjnego z możliwością zastosowania w sterowaniu mikroreaktorów.

W nanosieciach informacje są przenoszone poprzez odpowiedni stan poruszającej się molekuły. W komunikacji na mniejsze odległości (w zamkniętym obszarze ograniczonym granicą nanoprocesu) stan molekuły sygnalizacyjnej wymuszany jest poprzez wiązania chemiczne z inną molekułą lub wymuszany jest oddziaływaniem środowiska. Procesy te w nanosieciach biologicznych zachodzą w kaskadach transdukcji sygnałów, podobne występują w nanotechnicznych systemach informatyki. Procesy te rozpatrywane są w aspekcie fuzji kaskad. W ogólności, oddziaływania te prowadzą do przełączania konformacji molekuł. W pracy, ograniczając się do nanostruktur biokompatybilnych wprowadzono standardowy, formalny opis struktury, metodologię modelowania i symulacji zmian konformacji oraz zaproponowano hierarchiczny opis nanosieci przydatny w analizie przełączeń konformacyjnych. Metodyka badań symulacyjnych bazuje na algorytmach programowania dynamicznego, zmodyfikowanej metodzie Monte Carlo oraz nowym, dwufazowym algorytmie pozwalającym śledzić zmiany konformacyjne w trakcie tworzenia polipeptydu (algorytm Nascent Protein Folding). Rozpatruje się także koncepcję „macierzy lepkiej" stanowiącej podstawę wybranych nanotechnologicznych, dwufazowych procesów produkcyjnych.

ABBREVIATIONS

A	adenine
AHDL	analog hardware description language
ASIC	application specific integrated circuits
ATP	adenosine triphosphate
bp	base pair (in a nucleic acid)
C	cytosine
CAB	configurable analog block
CAD	computer-aided design
CAE	computer-aided engineering
cAMP	cyclic adenosine monophosphate
CIF	Caltech intermediate form (VLSI mask description)
CPLD	complex programmable logic devices
DDBJ	DNA Data Bank of Japan
DNA	deoxyribonucleic acid
DRC	design rules checker
DS	development system (evaluation board with tested chip)
DSP	digital signal processing
DXF	drawing exchange format
EBI	The European Bioinformatics Institute (United Kingdom) http://www.ebi.ac.uk/
EEPROM	electrically erasable programmable ROM
EMBL	The European Molecular Biology Laboratory. EMBL was established in 1974 to conduct basic research in molecular biology and is supported by seventeen countries including nearly all of Western Europe and Israel. http://www.embl-heidelberg.de/
Entrez	The text-based search and retrieval system used at NCBI for the major databases, including PubMed, Nucleotide and Protein Sequences, Protein Structures, Complete Genomes and others. http://www.ncbi.nlm.nih.gov/Entrez/index.html

EPROM	electrically programmable ROM (UV-erasable)
EUROPRACTICE	An integrated circuits prototype fabrication and low volume production service in Europe. EUROPRACTICE was launched by the European Commission in 1995 and provides low cost and easy access to ASIC prototype, multi-chip module (MCM) or microsystems small volume fabrication in order to stimulate academics and industry use ASIC solutions in new product development (Interuniversity Microelectronics Center – Belgium, Rutherford Appleton Laboratory – United Kingdom, and Fraunhofer Institut Integrierte Schaltungen – Germany). http://www.europractice.com/
FPAA	field programmable analog array
FPGA	field programmable gate array
FSM	finite-state machine
G	guanine
GDSII	The standard stream file format for transferring/archiving 2D graphical design data (VLSI mask description). http://www.artwork.com/gdsii/
GenBank	The GenBank is the NIH genetic sequence database, an annotated collection of all publicly available DNA sequences. GenBank is part of the International Nucleotide Sequence Database Collaboration, which is comprised of the EMBL from EBI, DDBJ, and GenBank at the NCBI. http://www.ncbi.nlm.nih.gov/Genbank/GenbankOverview.html http://www.psc.edu/general/software/packages/genbank/genbank.html
GFLOPS	giga floating point operations per second
GTP	guanosine triphosphate
GUI	graphic user interface
HDL	hardware description language
IPR	The Institute for Protein Research at Osaka University (Japan)
ITE	The Institute of Electron Technology (Warsaw, Poland) http://www.ite.waw.pl/en
IUCr	The International Union of Crystallography
IUPAC	The International Union of Pure and Applied Chemistry
IUBMB	The International Union of Biochemistry and Molecular Biology
LOCOS	local oxidation of silicon (oxide construction technique)
MEMS	micro electro mechanical systems
mmCIF	macro molecular crystallographic information file
MML	multiconductor metal line
MOSIS	The MOS Implementation Service. MOSIS (since 1981) is a low-cost prototyping and small-volume production service for VLSI circuits development (USA). http://www.mosis.org/
MPC	model prediction control

MPI	message-passing interface
mRNA	messenger RNA
MTL	multiconductor transmission line
NCBI	The National Center for Biotechnology Information (USA) http://www.ncbi.nlm.nih.gov/About/index.html http://www.ncbi.nlm.nih.gov/
NCBI-Entrez-Nucleotide	NCBI nucleotides database http://www.ncbi.nlm.nih.gov/entrez/ (/Nucleotide)
NCBI-Entrez-Protein	NCBI protein database. http://www.ncbi.nlm.nih.gov/entrez (/Protein)
NIH	The National Institutes of Health (U.S. Department of Health and Human Services, USA) http://www.nih.gov/about/
NIST	The National Institute of Standards and Technology (USA) http://www.nist.gov/
NMR	nuclear magnetic resonance
PDB	file format PDB (Protein Data Bank format)
PDB	The Protein Data Bank. The single international repository for the processing and distribution of experimentally determined three-dimensional macromolecular structure data. The PDB is managed by Rutgers, The State University of New Jersey, the SDSC at the University of California, San Diego, and the NIST. International participants in data deposition and processing include the EBI Macromolecular Structure Database group (UK) and the IPR at Osaka University (Japan). http://www.rcsb.org/databases.html, http://www.rcsb.org/pdb/
PUL	per-unit-length
RISC	reduced instruction set computer
RNA	ribonucleic acid
ROM	read-only memory
rRNA	ribosomal RNA
SC	switched capacitor (FPAA technology)
SDSC	The San Diego Supercomputer Center at the University of California, San Diego (USA). http://www.sdsc.edu/
SWISS-PROT	The protein sequence knowledgebase which strives to provide a high level of annotation (such as the description of the function of a protein, its domains structure, etc.), and integration with other databases (Switzerland). http://us.expasy.org/sprot/
T	thymine
TEM	transverse electromagnetic
tRNA	transfer RNA
U	uracil

UGA	unity-gain amplifier
ULSI	ultra large scale integration
VHDL	V[ery high-speed integrated circuits] HDL
VHDL-AMS	IEEE/VHDL 1076.1 standard for a general description language for Analog Mixed-Signal systems. http://www.hamster-ams.com/index2.htm
VLSI	very large scale integration

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